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ELECTROMAGNETIC EFFECTS OF ADVANCED PACKAGING

Boeing Defense and Space Group

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Advanced packaged technology devices are providing improved performance characteristics in airborne, spaceborne, and land-based tactical military operations. Modern packaging technologies are also contributing to improved commercial systems performance. With the proliferation of these systems, their densely populated electromagnetic environments can result in electromagnetic susceptibility threats from within the packaging as well as from external sources. As a consequence, it is important that susceptibilities to electromagnetic environments be addressed early in the design and that these considerations include packaging design as well as circuit design. This document is the final scientific and technical report submitted under the Electromagnetic Effects on Advanced Packaging Contract F30602-94-C-0085. The purpose of this contract is to assist the US Air Force Research Laboratory, Rome Research Site in determining electromagnetic effects on advanced packaged devices and in determining evaluation models to identify, predict, and minimize electromagnetic effects on the reliability of devices and systems. The work was performed at the Boeing Space Center in Kent, Washington.

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ABSTRACT

Advanced packaged technology devices are providing improved performance characteristics in airborne, spaceborne, and land-based tactical military operations. Modern packaging technologies are also contributing to improved commercial systems performance. With the proliferation of these systems, their densely populated electromagnetic environments can result in electromagnetic susceptibility threats from within the packaging as well as from external sources. As a consequence, it is important that susceptibilities to electromagnetic environments be addressed early in the design and that these considerations include packaging design as well as circuit design. This document is the final scientnfic and technical report submitted under the Electromagnetic Effects on Advanced Packaging contract F30602-94-C-0085. The puspose of this contract is to assist the U S Air Force Research Laboratory Laboratory, Rome Research Site in determining electromagnetic effects on advanced packaged devices and in determining evaluation models to identify, predict, and minimize electromagnetic effects on the reliability of devices and systems. The work was performed at the Boeing Space Center in Kent, Washington.

KEY WORDS

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GLOSSARY

ASIC	Application Specific Integrated Circuit
BIT	Built-in Test
CAD	Computer Aided Design
CAS	Column Address Select
CMOS	Complimentary Metal Ooxide Semiconductor
CPU	Control-Processor Unit
CW	Continuous Wave
DRAM	Dynamic Random Access Memory
DXF	Design Exchange Format
EM	Electromagnetic
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
FEM	Finite Element Method
MIM	Multi-layer Interconnect Modeler
MCM	Multi-chip Module
NMOS	Negative Metal Oxide Semiconductor
PIU	Processor-interface Unit
PMM	Processor-memory Module
PMOS	Positive Metal Oxide Semiconductor
RAS	Row Address Select
RF	Radio Frequency
RLC	Resistor - Inductor - Capacitor (filter)
SPICE	Simulation Program for Integrated Circuit Electronics
TAB	Tape Automated Bonding
TI	Texas Instruments
WE	Write Enable
3-D	Three Dimensional
3DMM	Three Dimensional (Stacked) Memory Module

1.0 INTRODUCTION

The Scientific and Technical Final Report is submitted to the Air Force Laboratory in accordance with CLIN 002, CDRL A005, of contract F30602-94-C-0085 "Electromagnetic Effects on Advanced Packaging" (EMEAP). The purpose is to describe the modeling and simulation that was performed, the test fixture that was designed and fabricated, the testing that was performed, and to report the results of the investigation performed under this contract.

1.1 Objective

The objective of this study is to determine, through modeling and evaluation, the high frequency electrical characteristics of several advanced packaged electronic devices and to discover design approaches of advanced packaging that contribute to successful packaging design. Although advanced technology devices provide improved performance characteristics, they also contribute to an environment that can create electromagnetic susceptibility threats from within the packaging as well as from external sources. It was also the objective of this study, to design and fabricate a conducted interference test fixture and to utilize the test fixture in the evaluation phase of the contract.

1.2 Approach

The approach taken in this study was to select and procure two types of advanced packaged devices, which were tested and modeled. Electrical models of the devices were created and electrical simulation was performed on the models to determine their calculated response to various test conditions. A test fixture, test adapters, and signal combiners were designed and fabricated. These fixtures were used to test the two devices. The modeling data was then compared to the test results to determine if the modeling and simulation had been correctly performed.

1.3 Summary

The Texas Instruments' three-dimensional memory module (3DMM) and the Boeing processor-memory module (PMM) were selected as the devices for analysis and evaluation. The test device design data files were converted into representations of the physical devices and then into electrical models of portions of the devices. Electrical simulation was performed using these models and the results are presented. A test fixture, signal combiners and test adapters have been designed and fabricated. Conducted susceptibility testing was performed on the 3DMM and the PMM. Susceptibility levels were determined for several different package pins at a number of different test conditions. A list of recommendations to be used during design of advanced packaged devices was developed and is presented at the end of the report.

2.0 IDENTIFICATION OF CANDIDATE DEVICES AND TECHNOLOGIES

A number of advanced technologies for electronic packaging have emerged in recent years. These include surface mount, multi-chip module, hybrid packaging, chip scale packaging, pin grid array, ball grid array, flip-chip, tape automated bonding, and other types of high-density interconnect packaging. The rapid advancement of packaging technologies has resulted in many new materials, techniques, and processing methods. Circuit density and interconnect density have both increased as designers try to put more circuitry into smaller areas. Digital devices, many of which require a large number of pins to implement their functions, have driven many of the high density interconnect package types. Various types of radio frequency devices have also utilized advanced packaging techniques, which has enabled higher frequency operation than the dual-in-line packaging so common throughout the packaging industry. In addition to different packaging techniques, there are different packaging materials, which could impact susceptibility performance. Hybrid packaging, which typically uses co-fired ceramic substrates with conductive inks or thick film construction techniques to carry the signals, utilizes metal packages with welded seams and glass to metal lead seals for high thermal conductivity and low moisture invasion. Ceramic packaging is also a relatively high thermal conductive package with low moisture invasion properties. Plastics, although not as good as hybrid or ceramic for either thermal or moisture properties, provide adequate physical protection and thermal performance in many applications for cost-conscious customers.

A stacked (three-dimensional) memory module (3DMM) produced by Texas Instruments (TI) and a processor-memory module (PMM) produced by Motorola and Boeing, were selected as the test devices. The selection process was made after reviewing a large number of devices with advanced packaging features. In addition to being fabricated using advanced packaging techniques, the selected test devices were available at reasonable cost, and design data was available in a form that appeared to support the modeling process.

2.1 Three Dimensional Memory Module (3DMM)

The 3DMM, which is shown in Figure 2.1-1, is a test unit specifically designed for the purpose of structural durability testing. It contains three dimensional (3-D) memory technology used by TI's Defense Systems and Electronics Group to build high density, state-of-the-art, silicon-on-silicon multi-chip modules, (MCMs). Each test unit includes two 3-D memory die stacks attached to a thin film multi-layer interconnect (substrate), which is also called the "die-re-route". A Kovar hybrid package was chosen to house the 3-D MCM to facilitate durability testing.

Each 3DMM die stack is made up of eight 1-megabit commercial dynamic random access memory (DRAM) devices (TMS44C2560) made by the Texas Instruments Semiconductor Group. The DRAM signals were extended to the long edge of the die using aluminum over titanium tungsten (Ti:W/Al), polyimide, and gold over titanium tungsten (Ti:W/Au). On-chip rerouting and gold solder bumps are added while the die is in wafer form. Tape automated bonding (TAB) is used to connect individual die to gold plated copper TAB tape. After electrical testing, the die is excised from the TAB tape frame and laminated together, eight at a time. The copper TAB leads extend from the bottom, as

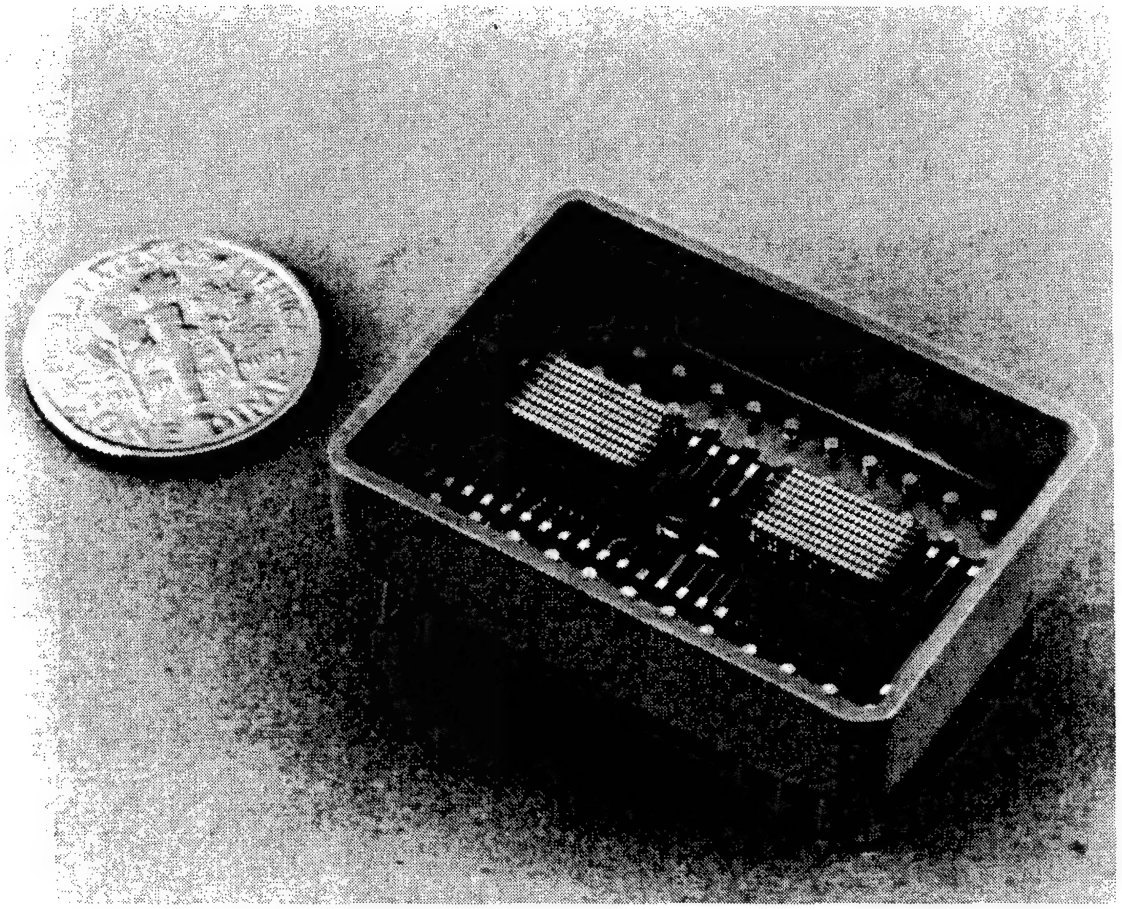


Figure 2.1-1, Three Dimensional Memory Module (3DMM)

well as the top of the stacks. The bottom side leads are used to attach the die stack to the interconnect. The topside leads are used for probing during failure analysis.

The interconnect is fabricated on a silicon wafer and consists of Ti:W/Al neutralization, polyimide dielectric layers, nickel solder pads for 3-D stack attachment, Ti:W/Au pads for wire bonds, and Ti:W/Au pads for capacitor mounts. The interconnect is designed to hold two 3-D die stacks and two bypass capacitors. The interconnect design busses all 16 DRAMs together by connecting all like signals except for the row address select (RAS) and column address select (CAS) signals. There are 49 signals routed to bond pads on two sides of the interconnect. The identification nomenclature for the 16 die is stack A or B, die 1 through 8.

The substrate, with the 3-D die stack and decoupling capacitors, is attached using epoxy, to a gold plated, Kovar, 50-pin, staggered lead bathtub package. A Kovar lid is welded to the package to

complete the hermetic seal. Some of the mechanical details of this package are shown in Figure 2.1-2 and a layout of the substrate in shown in Figure 2.1-3. 3DMM Package pinout information, routing information and a DRAM data sheet are shown in Appendix A. Gold wire bonds connect the substrate pad to the package posts. The longer wire bonds to the outside posts are approximately 180 mils in length. Although this exceeds Texas Instruments standard design practice, the focus of the development of this device is to produce the 3-D stacks and their interconnects. All test units, except for humidity test units, are hermetically sealed with a gold plated Kovar lid attached by seam welding. The humidity test units are not hermetically sealed in order to simulate commercial type products.

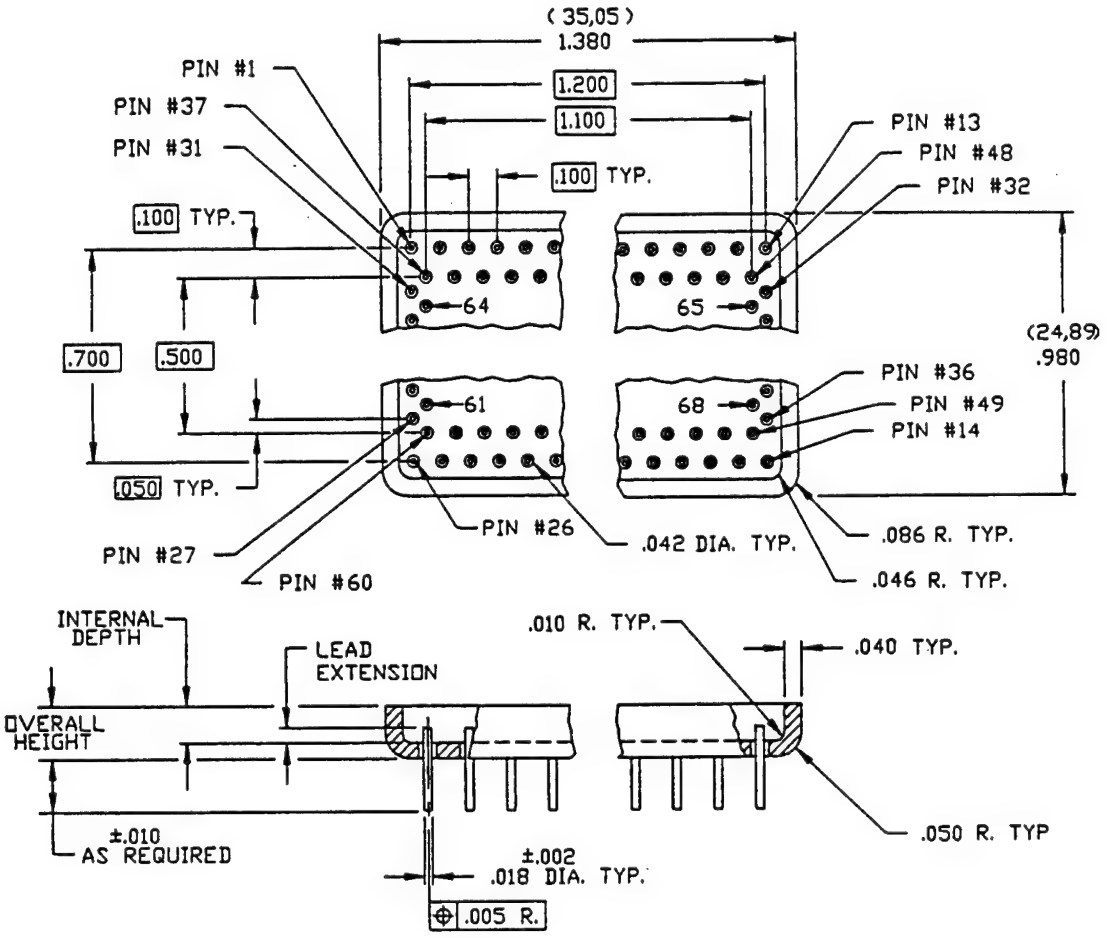


Figure 2.1-2: Mechanical details of the 3DMM package

2.2 Processor Memory Module (PMM)

The Processor Memory Module (PMM) was originally designed as a silicon-on-silicon MCM-D (deposited) process that was developed by Boeing. The current PMM design is based upon

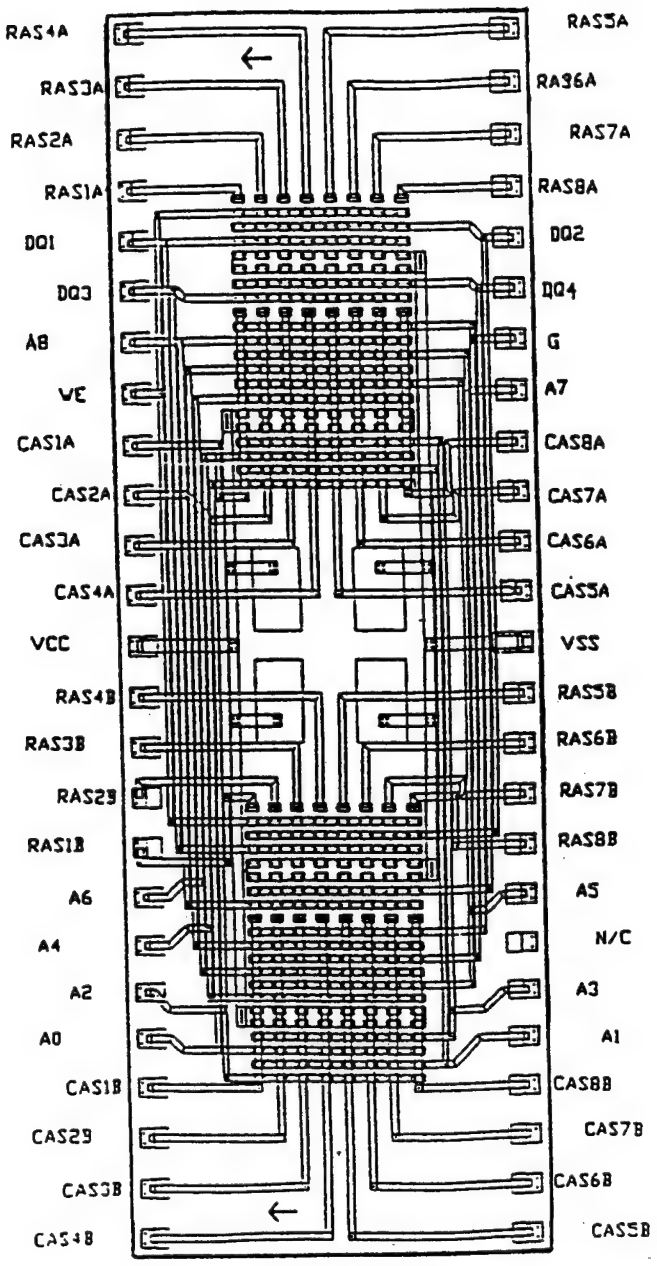


Figure 2.1-3: Layout of the 3DMM substrate

Motorola's MCM-L (laminated) substrate technology. It is a multi-chip module that uses plastic encapsulated integrated circuit dies. The signals from 130 critical internal test points are brought out for external electrical testing. The PMM built-in-test (BIT) design will support fault isolation and susceptibility diagnostics in electromagnetic effects testing. The PMM includes 7 static random access memory chips, 7 flash memory chips, a processor and another application specific integrated circuit (ASIC) chip. An expanded version of the device, called the "smart card PMM", includes additional logic for troubleshooting and a 140 connection edge-card interface through which the memory could be accessed without going through the ASIC and processor.

After acceptance testing of the "smart card" PMM, the portion of the circuit containing the troubleshooting provisions would be cut off and the PMM could be mounted as a "j-lead" surface mount package or in a Kovar hybrid package. The "smart card" PMM is shown in Figure 2.2-1. The photo-plot images of the 8 layers that make up the PMM laminated substrate are shown at approximately 155% of full size in Appendix B. Unfortunately, development of the PMM was cut short and a complete PMM, including the processor and ASIC, utilizing the MCM-L substrate, was never completed. A number of the memory-only PMMs, however, completed an extensive environmental test, and these were made available for our use on this research contract.

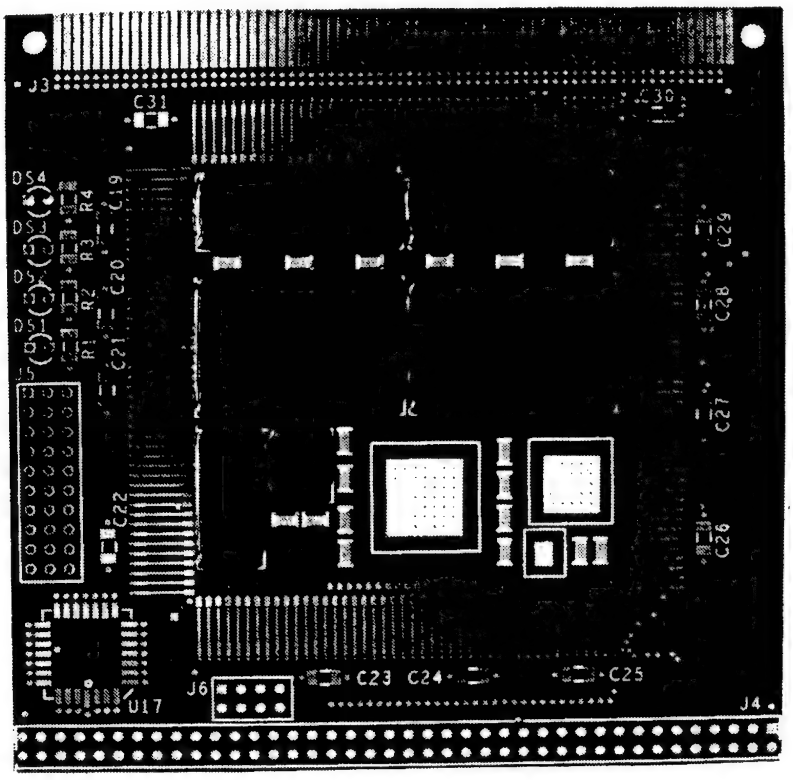


Figure 2.2-1: "Smart card" PMM

3.0 MODELING AND SIMULATION

The task of modeling electromagnetic effects in devices such as the PMM and 3DMM is composed of two separate sub-tasks. The first task is to model the passive portions of the devices, which designers in the past have typically thought of as simply part of the packaging. These passives include the pins, the circuit board traces, bond wires, package casing, etc. In this task the mechanisms which transport both desired and undesired signals between the device components will be identified.

The second task is to predict how the active device components will respond to the signals they receive. The task of modeling the coupling effects between signal paths can be performed by reducing the effects of the packaging geometry into an equivalent electrical circuit, which can then be analyzed using standard circuit analysis tools. The model thus created takes into account mutual and self capacitances and inductances of all the circuit paths. With this model, one can analyze how signals propagate between input pins and the active devices. There are a number of software tools available for performing such analysis. The tools we utilized for modeling the packaging geometry of the PMM are Ansoft's Maxwell Multi-layer Interconnect Modeler (MIM) and Autodesk's AutoCAD. The 3DMM modeling effort used the Ansoft Maxwell software and Contec's ContecPLANE software. It is interesting to note that the tools used in both the PMM and the 3DMM modeling efforts to extract electrical parameters from the geometry were unable to converge on solutions for models of somewhat reduced complexity, let alone for detailed models of the entire structures.

The task of simulating circuit response is performed using MicroSim's PSPICE© A/D, which is capable of both analog and digital simulation. PSPICE is a variation of University of California Berkeley's SPICE (Simulation Program with Integrated Circuit Emphasis).

3.1 Modeling of the Processor-Memory Module

The susceptibility model we have developed requires an accurate model of the inductive and capacitive parasitics of the input structure and its surrounding circuitry. The procedure used to extract those electromagnetic parasitics, which subsequently results in a functional SPICE sub-circuit for use in the continuing development of the final susceptibility model, is described below.

The level of accuracy needed for the susceptibility model requires a computer aided design (CAD) layout of the MCM input structure. Because Maxwell's 3D Solid Model file (SLD) model format is not directly compatible with most drawing file formats, two intermediate file formatting steps were required before the final model could be created. The original design data base for the PMM multi-chip module was not directly compatible with Boeing's suite of CAD tools, but we discovered that if the files were in Gerber®4 file format, they could be read and converted into files that are compatible with the existing drawing tools. Upon request, Motorola provided a Gerber®4 file of the surface layer of the PMM, which was converted to Drawing Interchange Format (DXF) format and subsequently imported into AutoCAD. The intermediate translation steps were cumbersome and tedious because of the need to fine-tune the model. But rather than detail the step-by-step model creation process, we will detail the issues of using these tools to create valid EM models for use in PSPICE or similar high level computer aided engineering (CAE) simulation tools.

Figure 3.1-1 shows several layers of a portion of the PMM. The complexity of the processor interface unit (PIU) chip and its interconnect does not lend itself well to Finite Element Method (FEM) modeling. This is due to fact that FEM processing time is directly proportional to the number of meshed nodes required to describe the model mathematically. To reduce processing to a reasonable

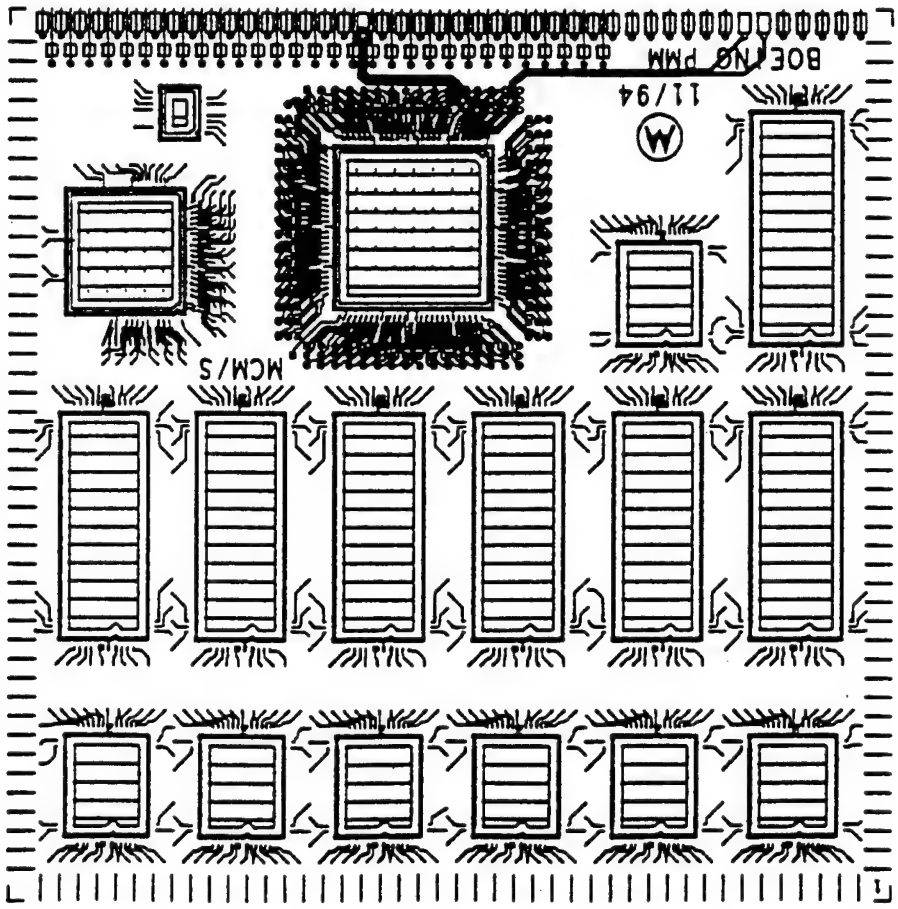


Figure 3.1-1: Several Layers of a Portion of the PMM

amount of time, the model was simplified to that shown in Figure 3.1-2. The simplification was intended to reduce CPU time by eliminating higher order effects that we expected to have minimal impact on the model. The FEM solver (Maxwell) would not converge on a mesh solution for this reduced complexity model, so the model was further simplified by removing most of the circuitry surrounding the area of the bond pads as shown in Figure 3.1-3. This greatly simplified model was finally able to converge on a mesh solution. Unfortunately, the portion of the PMM that was modeled here is not the same portion that was tested on the conducted susceptibility test fixture. As described in section 2.2, the development of the PMM was curtailed and a complete PMM, including the processor

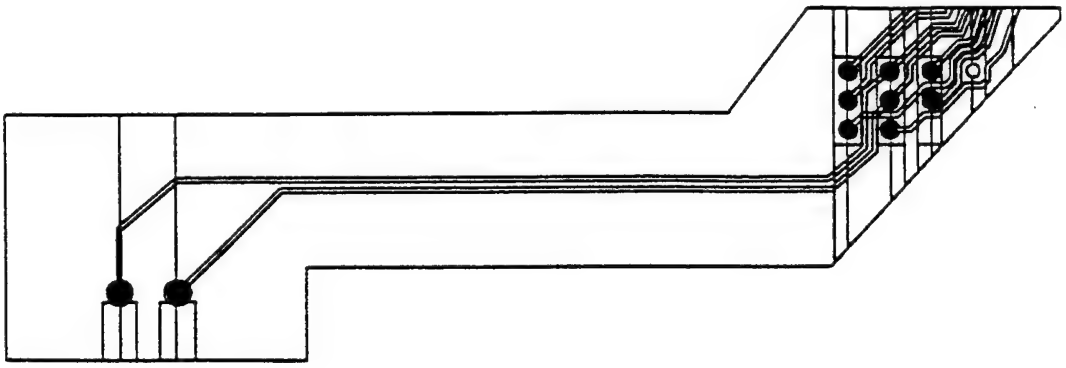


Figure 3.1-2: Simplified Model of a Portion of the PMM

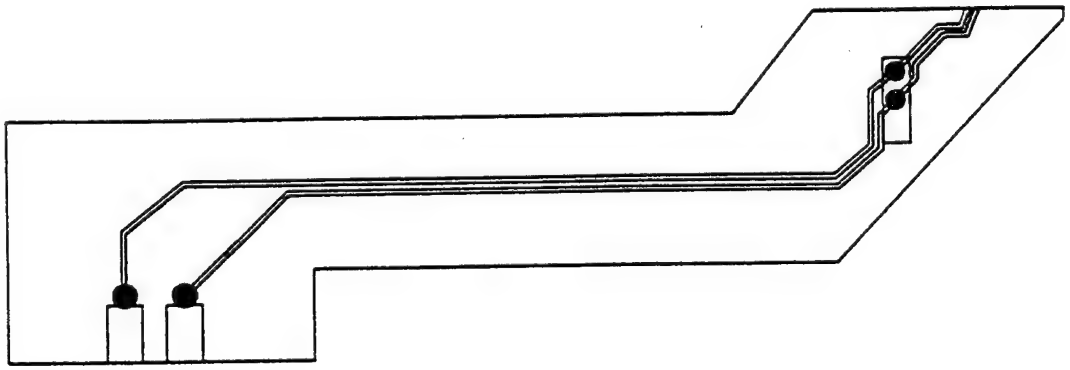


Figure 3.1-3: Further Simplified Model of a Portion of the PMM

and ASIC, was never completed. The PMMs we received were memory-only devices and did not have the ASIC or controller installed.

Some modeling was done in SPICE to determine which device parameters affect sensitivity to electromagnetic interference (EMI) and to quantify the results. A lumped element model of two traces on the PMM was combined with a model of an input buffer composed of a pair of CMOS inverters. A pulse with a nominal risetime of 0.2 ns was fed to one of the traces, which led to the input stage of the buffer. A radio frequency (RF) source was placed on the other trace, which was assumed to be terminated at the other end with a 50-ohm load. The ability of PSPICE to perform parametric analyses on this model can be used to determine the sensitivity of the model to changes in any of the parameters. In this modeling study, the gate width of the positive (PMOS) and negative (NMOS) channels in the CMOS devices was allowed to vary by a factor of 0% to 10% (from 1.0 to 1.10). If both the PMOS and the NMOS gate widths varied in the same direction, there was no net effect on the rise-time of the output pulse. However, if the PMOS gate widths were allowed to increase while the NMOS gate widths decreased, the risetime changed. This effect is illustrated in Figure 3.1-4. If the PMOS widths

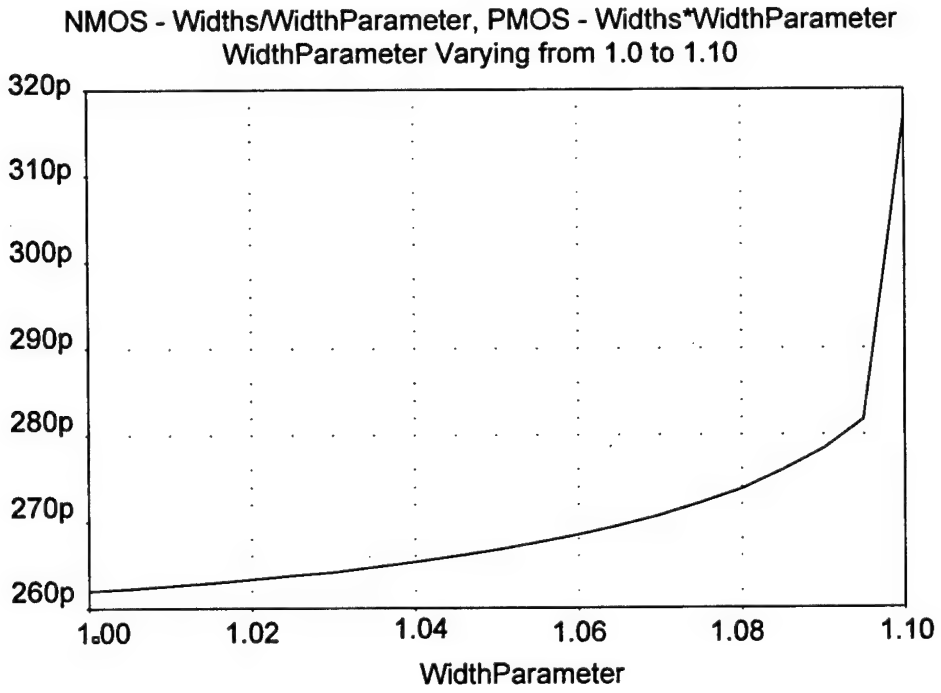


Figure 3.1-4: Simulation of Risetime vs. NMOS & PMOS Gate Width Parameter

decreased while the NMOS gate widths increased, a different pattern emerged. This is shown in Figure 3.1-5. In another modeling analysis performed on a similar PMM circuit, PSPICE was utilized to examine variations in the input parameters. In this analysis the phase of the RF noise coming into the device input was varied from 0° to 180° with respect to the digital signal leading to the buffer. A plot of how the rise-time of the output pulse was affected by the changing phase is shown in Figure 3.1-6.

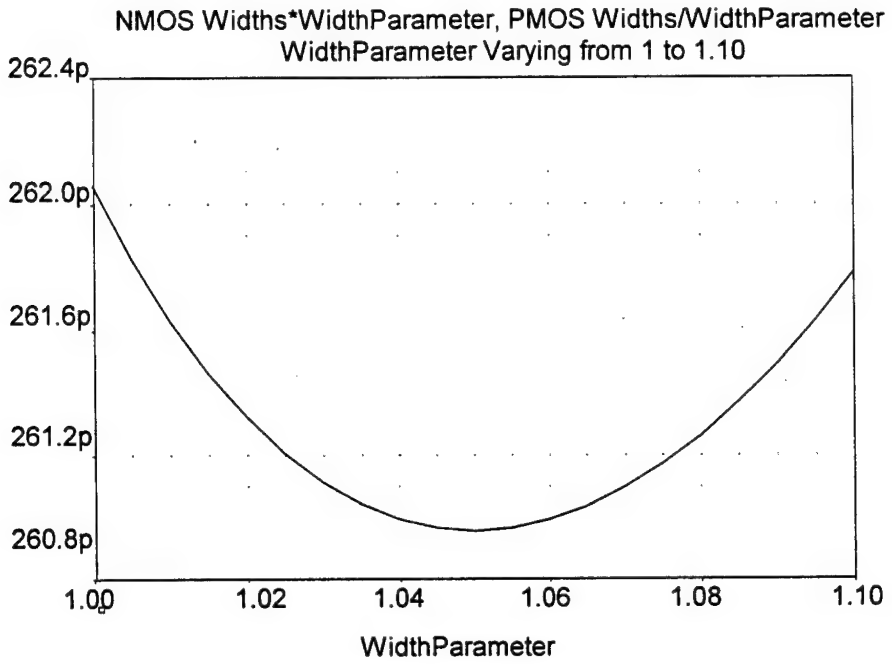


Figure 3.1-5: Simulation of Risetime vs. NMOS & PMOS Gate Width Parameter

3.2 Modeling of the Three Dimensional Memory Module

The 3DMM, which is shown in Figure 2.1-1, has a very complex mechanical and electrical structure. To extract its electrical equivalent model, the 3DMM was divided into five subsystem elements: package pins, bond wires, substrate, die reroute, and die. To keep the model from becoming overly complex, only selected signals were modeled. These signals included write enable (WE), data in/data out line #3 (DQ3), the negative supply voltage (Vss), the positive supply voltage (Vcc), Column-address strobe (CAS), and row-address strobe (RAS). Lines were modeled for four of the sixteen die: 4A, 5A, 3B, and 6B. These signals were chosen because they were among the signals with the longest trace lengths. A total of 12 signals on the substrate were modeled. An electrical equivalent circuit for each subsystem was generated and then integrated into the final model.

Ansoft 2D was used to extract the parametrics of the package pins. Mutual inductance and capacitance between the modeled package pins was assumed to be a second order effect and not included in the model. The pins are 20 mils in diameter and 320 mils long and are made of Kovar. Ansoft 2D was also used to extract the parametrics of the bond wires. The mutual terms were again assumed to be a second order effect and were not included in the model. The bond wires are gold and are 1 mil in diameter.

The substrate signals were modeled taking into account the interaction with the metal case. The absence of a ground plane in the substrate makes the case an integral part of the way signals are propagated in the system. The negative supply voltage (Vss) pin is also electrically connected to the case. ContecPLANE was chosen as the modeling software because of its ability to model ground planes

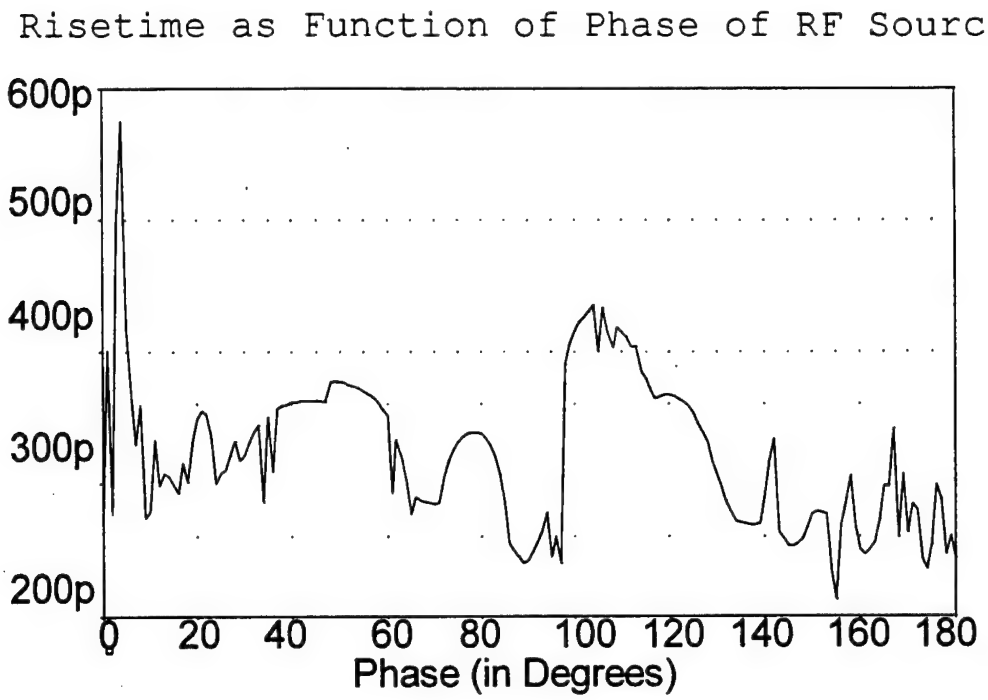


Figure 3.1-6: Risetime of an Inverter Gate vs. Phase Noise

as return paths, rather than simply 0-volt ground references. The software extracts resistance and inductance only. Capacitance values were generated independently and integrated into the model. The case was modeled as a solid sheet with 7 reference ports on the plane. These reference ports establish the SPICE program nodes that are then hooked up to other segments of the circuit models. The lines, as etched into the substrate, are 0.12 mils thick and are 8 mils wide for signal runs and 12 mils wide for power runs. Figure 3.2-1 shows the top view of the substrate.

The die reroute is a polyimide based structure with two metal layers that route the die input/output traces located on the short edges of the die to the bottom of the die for attachment to the substrate. The Ansoft Maxwell EM software was used to extract the electrical parameters from this structure. This structure has a number of parallel lines that have right angle bends that necessitated a 3-D approach to modeling. The physical model was set up and an attempt was made to generate the resistor-inductor-capacitor (RLC) matrix. After a number of unsuccessful attempts to run the model, it was determined that the complexity of the model made the solution virtually impossible to accomplish unless the model was simplified. At this point it was decided to concentrate only on signals that were most critical to the memory operation. The signals chosen were Vcc, Vss, write enable (WE), CAS, RAS, and DQ3. Vcc and Vss were chosen because they are the power supply and ground reference. WE, CAS, and RAS control critical timing on the die. DQ3 was chosen as a representative data line because it is the longest data line and is farthest from ground. After simplifying the model, the software was able to extract an RLC matrix. A PSPICE model was then generated for this geometry. Figure 3.2-2 shows the Ansoft geometry model.

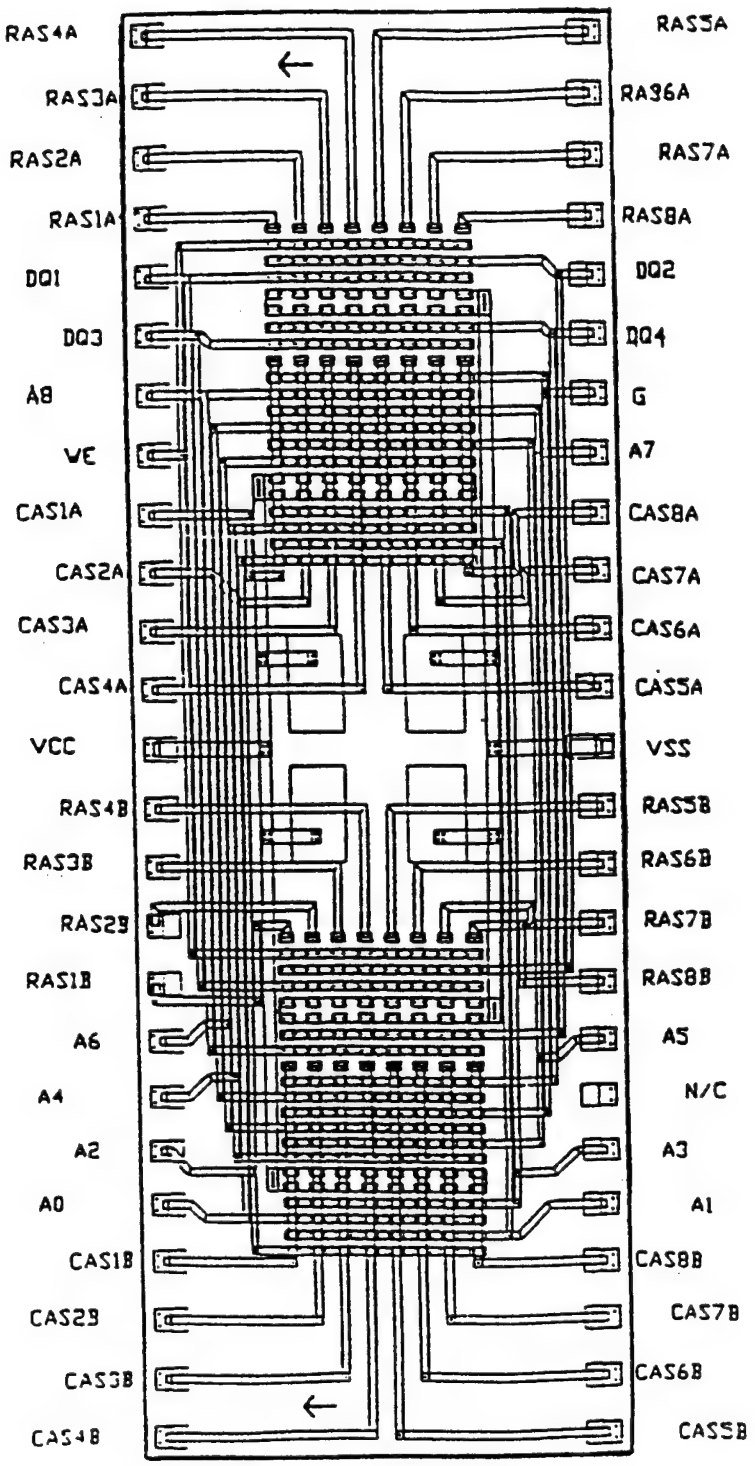


Figure 3.2-1: Circuit Layout of 3DMM Substrate

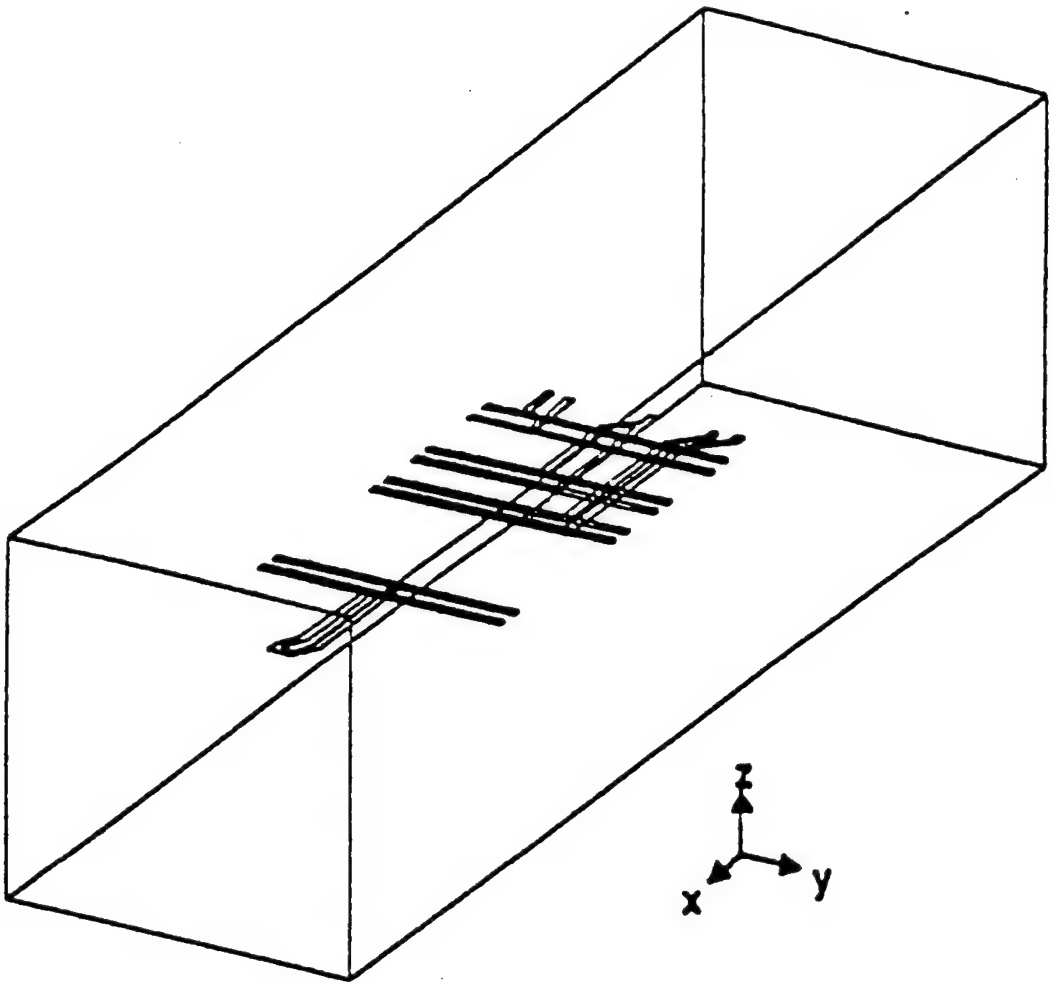


Figure 3.2-2: Ansoft geometry model

The die were modeled using a very simple input gate arrangement for the four input signals modeled on each die. Actual models for the Texas Instruments dynamic random access memory (DRAM) are available only in TISPICE and are not compatible with PSPICE. The simple models provided give a fairly accurate model for input impedance.

Although the frequencies of interest for this project extend to 18 GHz, the modeling software used only gives a solution for one particular frequency. For this effort the problem was solved at three frequencies: 100 MHz, 10 GHz, and 18 GHz. At these frequencies the resistance of the etched lines

varies at approximately the inverse of the square root of the frequency. A separate PSPICE model was generated for each of the frequencies under consideration.

The five subsystem models were integrated into the final PSPICE models for the 3DMM. Each of the three PSPICE model files for 100 MHz, 10 GHz and 18 GHz, were arranged in similar fashion. The nodes were named using a convention that distinguishes the five subsystems. The first section of the files contains the various stimuli. These can be varied at the user's discretion depending on what type of stimulus is necessary for simulating a particular noise input into the circuit. The next section contains the input pin models, which includes a model of the pin for each of the 12 signals in the bond wire section. These 12 signals are followed from the pin to the substrate. The nodes are referenced to the nearest ground point on the package. The next section is the sub-circuit for the substrate and case, which contains 57 nodes. The first 7 nodes are Vss nodes. These connect the Vss input at the substrate to the 4 memory die in the model and the 2 capacitors. The next 7 nodes are the Vcc nodes and they are hooked up like the Vss nodes. The next group of 7 nodes are the ground references to the case. The remainder of the nodes is the various WE, CAS, RAS, and DQ3 lines that are routed to the memory die. The next section is the die overlay model. The Vss and Vcc inputs have two connections at the substrate interface and one at each die. This provides a lower resistance parallel path to the die. The next section is the memory die, and it is composed of 4 input gates per die along with Vcc and Vss connections. The gates are inverting so that the output can be monitored for upset. The last section includes the various commands for analysis and probing. The ".INC" statement references the substrate subcircuit and should be changed to the path name where this file is located. The ".TRAN" and ".AC" lines can also be changed or commented out depending on the type of analysis being performed.

The input stages of the active devices from the Texas Instruments 3DMM are the only PSPICE models that were created under this effort. A number of different input stimuli can be applied to the circuit, depending on the type of electromagnetic interference studies being conducted. For this report a limited number of stimuli were applied. The analysis focused on a 1-volt noise source, applied from 100 MHz to 20 GHz, entering the package data line DQ3. Figure 3.2-3 shows the voltage level of the signal DQ3_6BD, which is the memory die 6B pad, and it has virtually no attenuation at 100 MHz. An AC PSPICE run was also made at three frequencies, 100 MHz, 10 GHz and 18 GHz, so the response can be seen in finer detail. Figures 3.2-4, 3.2-5, and 3.2-6 show the voltage level of the signal DQ3_6BD, which is at the memory die 6B pad, at those three frequencies. Figure 3.2-4 shows virtually no attenuation at 100 MHz. It would be expected any noise in this frequency range would be seen at full voltage at the die. Figure 3.2-5 shows the response in the 10 GHz frequency range, where the 1 volt signal on DQ3 is attenuated by roughly 60% (-4 dB) as it progresses through the package. The signal at the die is actually of greater magnitude than the signal on the substrate. This may possibly be a resonance on the memory overlay circuitry. Figure 3.2-6 shows the signal at the 18 GHz, where the signal at the die is only about 100 microvolts (40 dB down from the original signal).

The conclusions we reach from this simulation are the following: For upset to occur at the die, noise signals of sufficient amplitude must be propagated from outside the package through the internal circuitry and onto the die. For TTL level logic, this voltage is generally considered to be 0.8 volts. The package geometry will transfer energy very well at the 100 MHz frequency range. A signal level of 0.8

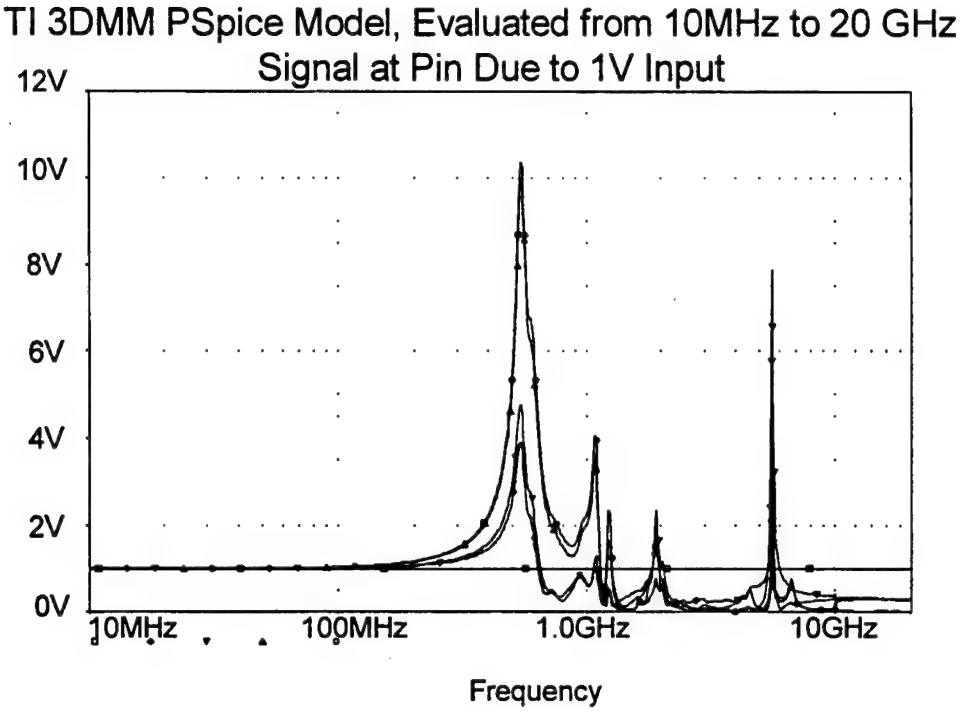


Figure 3.2-3: PSPICE Simulation of DQ3_6BD from100 MHz to 18 GHz

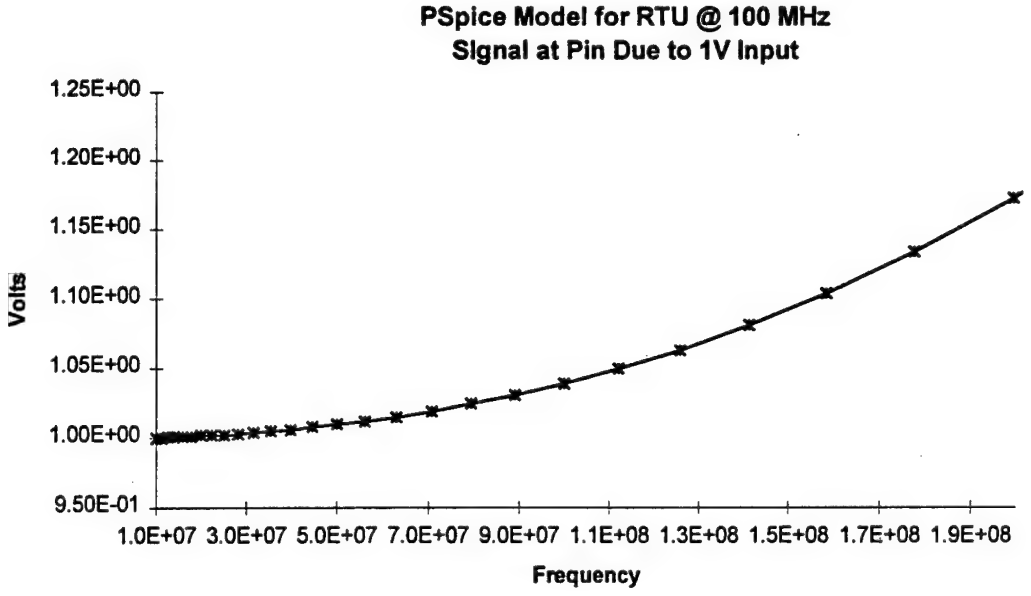


Figure 3.2-4: PSPICE Simulation of DQ3_6BD at 100 MHz

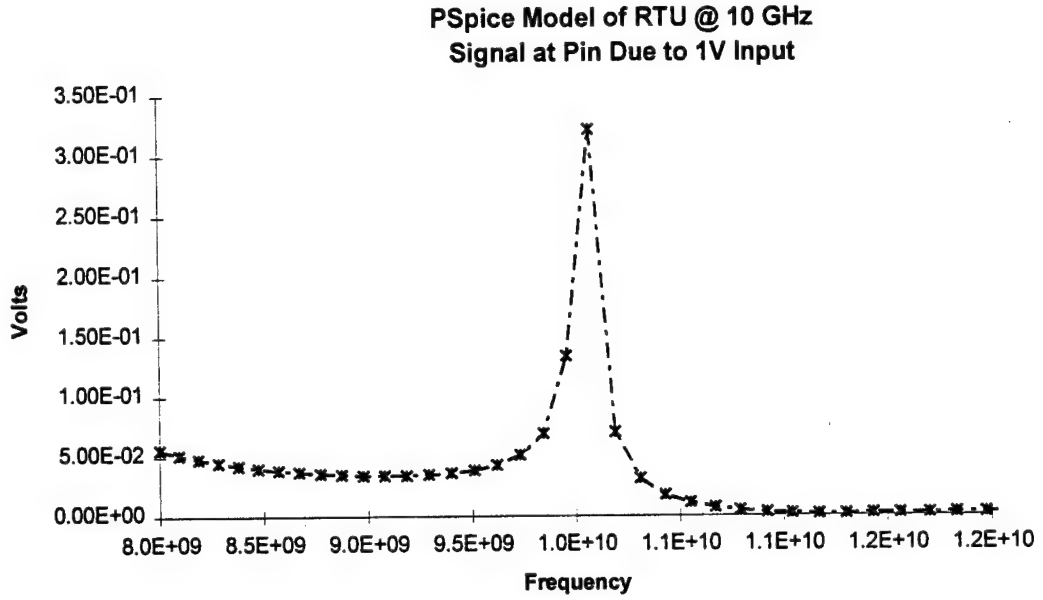


Figure 3.2-5: PSPICE Simulation of DQ3_6BD at 10 GHz

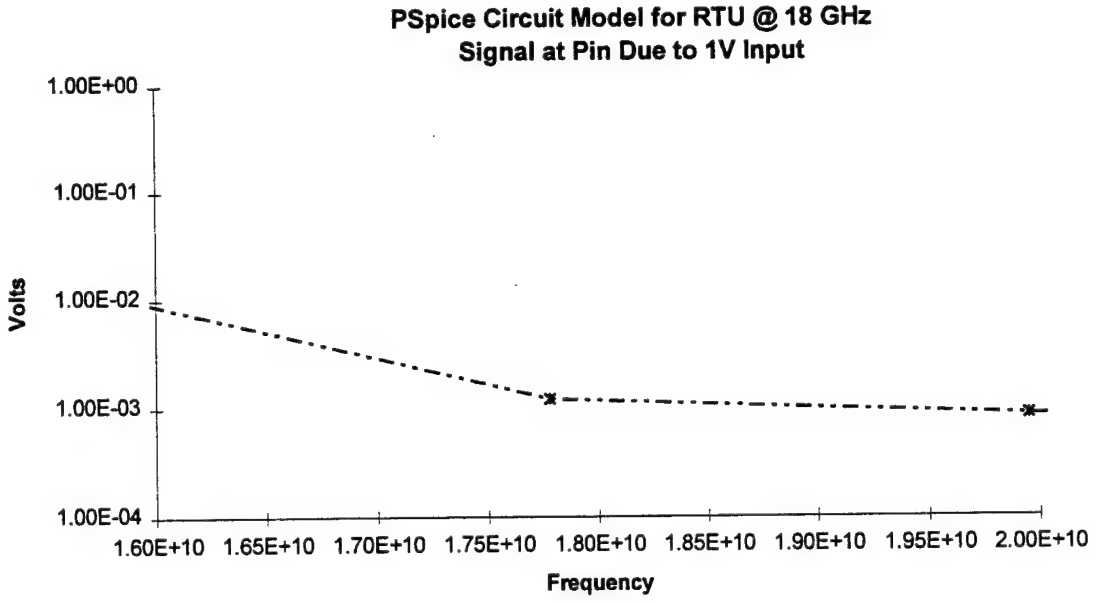


Figure 3.2-6: PSPICE Simulation of DQ3_6BD at 18 GHz

volts is normally large enough to cause upset at the die level. Even at 10 GHz the level of noise transferred to the die is significant, only 4 dB down. A 1-volt signal would be of sufficient amplitude to cause noise concerns. But at 18 GHz the level of noise would have to be 4000 Volts to propagate a 0.8 volt signal to the die. The frequencies most likely to cause significant problems would be in the 100 MHz to 10 GHz region at amplitudes of 0.8 to 1 volt. Signals at 18 GHz would be sufficiently attenuated by the package parasitics and should not pose a problem to the packaged devices unless the package was being exposed to extremely high voltage signals.

3.3 Modeling Summary

A number of things were discovered in the process of modeling and attempting to model the two electronic test devices chosen for this program. We thought we were using the latest revisions of most software, but in some cases we did not, and this may have caused some of the problems that we experienced. In the case of the Auto-Cad, our copy was somewhat dated, and its output was not directly compatible with Ansosft Maxwell, but required an intermediate translation before the data could be used by Maxwell. The newer Windows version of Auto-Cad was compatible with Ansoft Maxwel and would have allowed us to eliminate the time-consuming translation step. When attempting to model the electronic devices, the electronic design data was available to us, but it was not in the form that was required as an input to the modeling program. The modeling program we were using, Ansoft Maxwell, did not have a very friendly user interface. A front-end processor that would allow data of different formats such as DXF, Gerber, etc. would have alleviated this problem. We also discovered, in our attempts to simulate the behavior of the advanced packaged devices, that the modeling software was not able to do what it promised to do, or at least what we expected it to do. For instance, because of the thin copper and dielectric structures involved in the multi-layer laminated circuit boards of the PMM, the aspect ratio (length vs. depth) of the structures was so high that the mesh granularity had to be very small, which made the 3-dimensional mesh structures extremely large. The modeling program never could converge on a solution until the size of the mesh was reduced to the point that the circuit elements were nearly trivial in scope. In reference 6 Howard Johnson, a well-known author of digital design and electromagnetic compatibility (EMC) related work, says that real-life EMI problems are much too complex for even the best software tools. We found this to be the case, especially in the area of converting a physical model to an electrical model. In retrospect, too much time was spent trying to integrate the various parts of the modeling and simulation part of the contract. Mr. Johnson also recommends that: 1) because the process involves 3D wave simulation (or modeling) over a large area, the computer will spend a lot of time to get even the most rudimentary results; 2) every bit of metal in the product matters, and many times the parts we might exclude in our model may turn out to be the ones that create the worst EMI headaches; and 3) because EMI is a strong function of switching speed, data patterns, and precise data timing, we would have to model any software that is running, including all possible combinations of software interaction.

4.0 CONDUCTED SUSCEPTIBILITY TESTING

Conducted susceptibility testing of the 3DMM and PMM was performed in the Boeing parts test laboratory in Kent Washington. The testing was conducted using an Advantech T3381 automated test system, the EMEAP test fixture and signal combiners described in sections 6 and 7, and general purpose test equipment. The Advantech T3381 is a digital integrated circuit test system. It contains 192 digital signal channels, 4 precision power supplies and an algorithmic pattern generator for testing memory devices at frequencies to 100 MHz (200 MHz multiplexed). The major parts of the Advantech T3381 are the processing unit, test head, and operator control interface. The processing unit consists of 9 full height racks of computing equipment. The operator control interface consists of a control and display panel on the test head, and a workstation terminal for programming, program execution, and status display. The test head contains the driver and receiver circuits that are necessary to interface to a multitude of different test devices, and it also performs preliminary processing of the test signals. Different test devices may be accommodated on the Advantech test head through the use of different test adapter boards. The test adapter boards make electrical contact with spring loaded pins in the test head. Two Advantech test adapter boards were customized for the 3DMM and the PMM by connecting test sockets and cables to the boards. These modified test adapter boards can be used to test the 3DMM and PMM directly or to test them through the EMEAP test fixture.

The 3DMM and PMM were tested by the Advantech before being subjected to conducted susceptibility testing in the EMEAP test fixture. In addition to the test hardware, general-purpose test equipment and test software are required to set up the Advantech to run a particular test and to provide test power to the signal combiners and RF test signals to the devices under test. The general purpose test equipment used for both the 3DMM and PMM tests are listed in Figure 4.0-1. The test software sets up the proper connections through the test adapter board to the test article, sets up the clock speed, and determines the signals that will be sent and monitored. After sending the appropriate signals, the Advantech will then place some of its signal lines into the listen mode and wait for correct signals to be received. For example, after sending a read signal with the appropriate chip select and addressing commands, it will be set up as a receiver to read the contents of a particular memory location. Figure 4.0-2 shows the Advantech test head, the Advantech test adapter board, the EMEAP test fixture, and some general-purpose test equipment during testing the PMM. The instructions for operating the EMEAP test fixture are given in Appendix C.

4.1 Testing of the 3DMM

The 3DMM test sequentially evaluates each of the 16 dynamic random access memory (DRAM) chips it contains. It tests one of the chips by holding all except one pair of the row address and column address signals inactive. When refresh cycles are required, all 16 DRAM are refreshed simultaneously. For each DRAM, the T3381 applies a memory test algorithm known as MATS++, which detects all possible address decoder faults, stuck-at (X) faults, and transition faults. A 50-pin quad in-line connector and cable assembly was soldered to an Advantech test adapter board to be able to test the PMM.

A test program was written for the 3DMM, and a program listing is contained in Appendix D, pages D1 through D19. The pin-out for the test is shown on pages D20 and D21. A subroutine, MATS, which is called a number of times in the main program, is listed in pages D22 to D38. The program is written in Fortran-like code that is proprietary to Advantech. Once the test program was ready, the 3DMM was inserted into the socket in the Advantech test adapter and tested. It passed most of the tests at a clock speed of 2.5 MHz. This is the first time we have tested the 3DMM, and our test engineer discovered that one of the 16 chips in the module did not respond. We had in our possession 3 good 3DMMs and 2 that were suspected to be bad, and all 5 of those showed that the chip select connection

EMEAP Susceptibility
Test Equipment Log

Test Articles: 3DMM & PMM_____ Part No.: _____
EWA No.: _____ Serial No.: _____
Control Doc.: _____ Test: _____

Model Number	Description	Manufacturer	BEHC Number	Cal. Date	Verify
436A	Power Meter	HP	10218482	6/22/98	X
8116A	Pulse/Function Generator	HP	30254345	4/1/98	X
1277H09 F000	TWT Amplifier	Hughes	30245836	6/7/91	X
20C4.0-8.0Q60	TWT Amplifier	Alto Scientific Co	10321651	NC	
VZS6951 F2	TWT Amplifier	Varian	10569920	NC	
HR-40-10	Power Supply	Systron Donner	30245398	NC	
HR-40-10	Power Supply	Systron Donner	10239564	NC	
8341B	Synthesized Sweep Generator	HP	30255951	6/21/98	X
8482A	Power Sensor	HP	07183094	6/6/97	X
8481A	Power Sensor	HP	02011896	7/26/97	X
8491B	Attenuator, 10 dB	HP	02003748	12/20/98	X
8491A	Attenuator, 6 dB	HP	1X734757	5-9-98	X
8491/b	Attenuator, 6 dB	HP	02010998	5/19/97	X

Figure 4.0-1: General Purpose Test Equipment used for 3DMM and PMM Tests

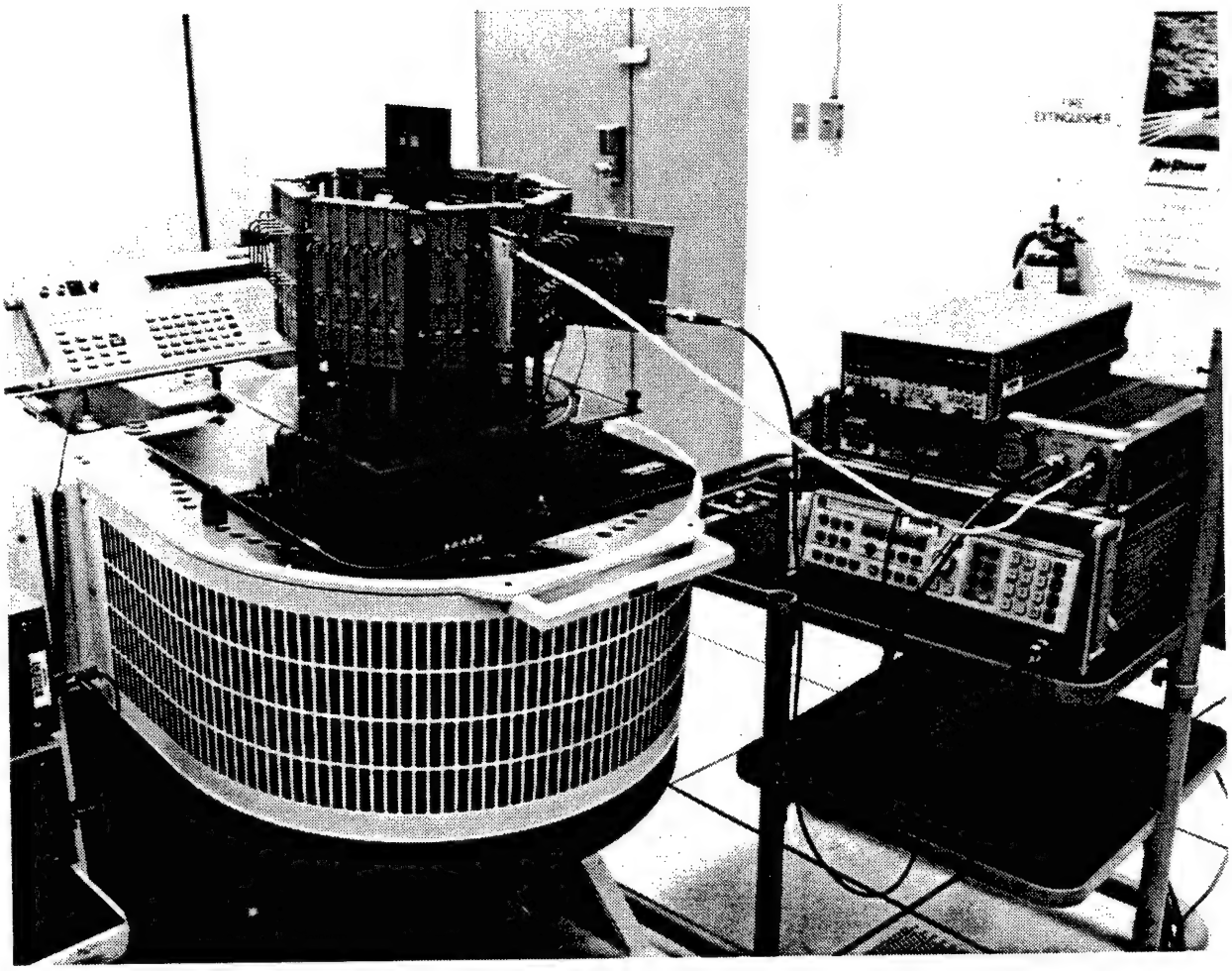


Figure 4.0-2: Photograph of Advantech Test Head During PMM Test

to memory chip "8B" was open. It is also interesting that one of the modules given to us and assumed to be non-functional actually works fine. Because of the non-functional memory chip, the test program was modified to test only the 15 good memory chips.

After the 3DMM test program was modified to account for the bad connection in the 3DMM, the EMEAP test fixture was placed on top of the Advantech test head and test adapter board. The EMEAP test fixture was connected to the test adapter board using a cable that was fabricated for that purpose. The 3DMM was plugged into the top of the test fixture, all of the through-signal adapters were attached to the test fixture, and the test program was run again. The test program failed at 2.5 MHz, and after several tries at frequencies below 2.5 MHz, the test passed at a clock speed of 500 kHz, which became the test frequency for the 3DMM when tested in the EMEAP test fixture.

Once the test program ran with the test fixture in place, we selected a signal line to test. For the modeling simulation of the 3DMM performed at Texas Instruments, data line #3 (DQ3) was modeled. In order to do a comparison between the simulation and the test, we tested the same data line. DQ3 comes from package pin 31 and goes to all 16 chips. We inserted a diplexer signal combiner into the EMEAP test fixture in series with this signal, and verified correct operation of the test program with no external RF signal applied. The output from an HP 8341B RF signal generator was then connected to the interfering signal input of the diplexer, and a 1 GHz signal was applied to the test article. The RF power level was increased until the signal generator's maximum output of 100 mw (+20 dBm) at 1 GHz was reached, and the test still passed. We added a TWT amplifier to the signal generator output and increased the signal level until the 3DMM test failed. After additional testing it appeared that the test would pass at an RF signal level of +25 dBm (about 0.32 Watt) and below and fail at an RF signal level of +26 dBm (about 0.4 Watt) and above at 1 GHz. The RF power was removed from DQ3 and a high power operational amplifier combiner was placed in series with the Vcc line, which is package pin 38. We used a 1 MHz sine wave for the interfering frequency, monitored the interfering signal at the test fixture input pin using an oscilloscope, and the voltage of the interfering signal was increased until the 3DMM failed its test. The test failure occurred at about 2.4V peak-to-peak (p-p) (1.2 V peak) above the 5 volt Vcc power supply voltage, while the test passed at 2.0 V p-p.

The interfering signal to the power supply line was turned off, and the 1 GHz interfering signal to DQ3 was energized again. We established the susceptibility level for DQ3 as +30 dBm (1 Watt RF) then reduced the RF power to +29 dBm at DQ3. This is about 5 dB higher than indicated by the first test. This difference could have been due to insufficient warm-up time for the equipment or the tester. Then we energized a 1 MHz interfering signal on the Vcc pin. With the RF power on DQ3 at +29 dBm the test failed if the 1 MHz signal on the Vcc was more than approximately 200 mv. RF power at DQ3 was reduced to +28 dBm and test failed when the interfering signal on Vcc was approximately 900 mv. With RF power to DQ3 lowered to +27 dBm the susceptibility level of the Vcc power supply was now approximately 1500 mv. The results of this testing are shown in Figure 4.1-1. As a result of this testing, it appears that the effect of separate sources of electromagnetic energy on this test device is somewhat cumulative, especially if there is coupling between the circuits. Because the Vcc powers every active circuit in the test device, noise or an interfering signal on the Vcc line should couple to the data lines. If an interfering signal is being impressed upon a circuit, but the signal level is below its susceptibility level, an interfering signal that is impressed upon another circuit, which is also below its susceptibility level, might be strong enough to cause device upset. In effect, each signal is below it's normal susceptibility level, but the cumulative effect is likely to result in susceptibility.

Once this testing was completed, additional testing was performed at lower frequencies in an attempt to validate some of the modeling and circuit simulation that had been done. Testing was done on line DQ3 with the diplexer signal combiner at frequencies between 100 KHz and 700 KHz. At 100 KHz the test just failed at 31.3 dBm, and at 200 KHz we did not experience any failures at power levels as high as +43 dBm (20 Watts). At 500 KHz the test failed at +32.8 dBm and at 700 MHz it passed at power levels as high as +43 dBm. Then we switched to a high-speed operational amplifier combiner and at 50 KHz with a +41 dBm signal the test passed, which means that we found no susceptibility at

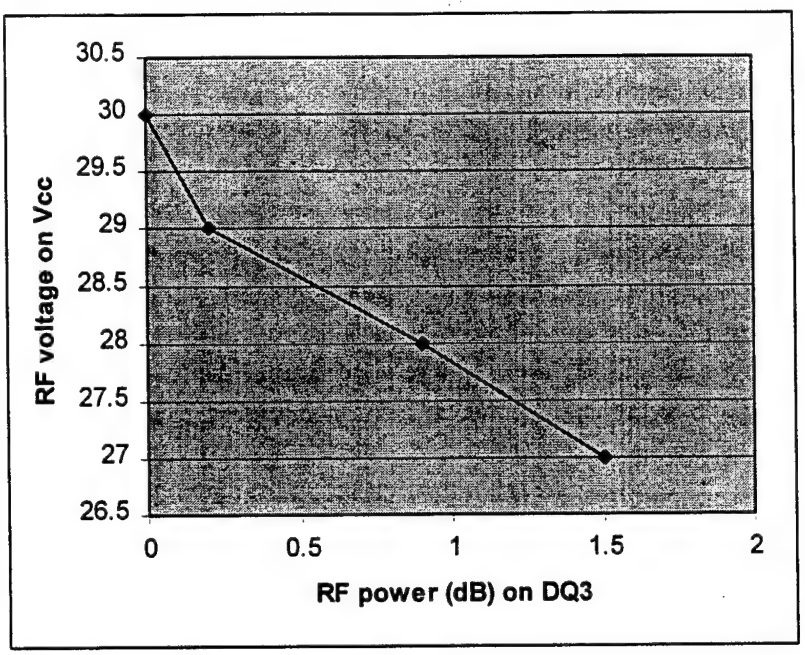


Figure 4.1-1: Susceptibility Level of 2-Signal Test on 3DMM

that power level. The test data sheets from the 3DMM conducted susceptibility testing are shown in Appendix E. The results of this testing are summarized in paragraph 4.3.

4.2 Testing of the PMM

A 140-pin edge-board connector and cable assembly was soldered to an Advantech test adapter board to be able to test the PMM. A test program has been written for the PMM, and a program listing is contained in Appendix F. To check out the PMM by itself, the test adapter board was placed on the Advantech test head and the test program was run. After a successful test was achieved, the EMEAP test fixture was placed on top of the Advantech test head and test adapter board, and the test cable was plugged into the bottom of the EMEAP test adapter. The EMEAP test fixture was prepared for the test by plugging one of the three sets of EMEAP test adapters into the top and bottom boards of the test fixture. The PMM was plugged into the top test adapter, and the general-purpose test equipment was added as required. Figure 4.2-1 shows the Advantech test head, the Advantech test adapter board, the EMEAP test fixture, and the PMM sitting in its test adapter board on top of the test fixture.

The PMM test sequentially evaluates each of the 7 static random access memory (SRAM) chips and 2 groups of the 7 Flash electrically programmable read only memory (EPROM) chips. Isolation of a test failure to a single SRAM or EPROM is complicated by the fact that the interface control signals are common among all 7 devices of each type. Therefore, the chips could not be operated individually. Fault isolation to a single SRAM was accomplished by holding the data input lines at the "erased" level for 6 devices, while testing the seventh. The SRAM devices were tested using

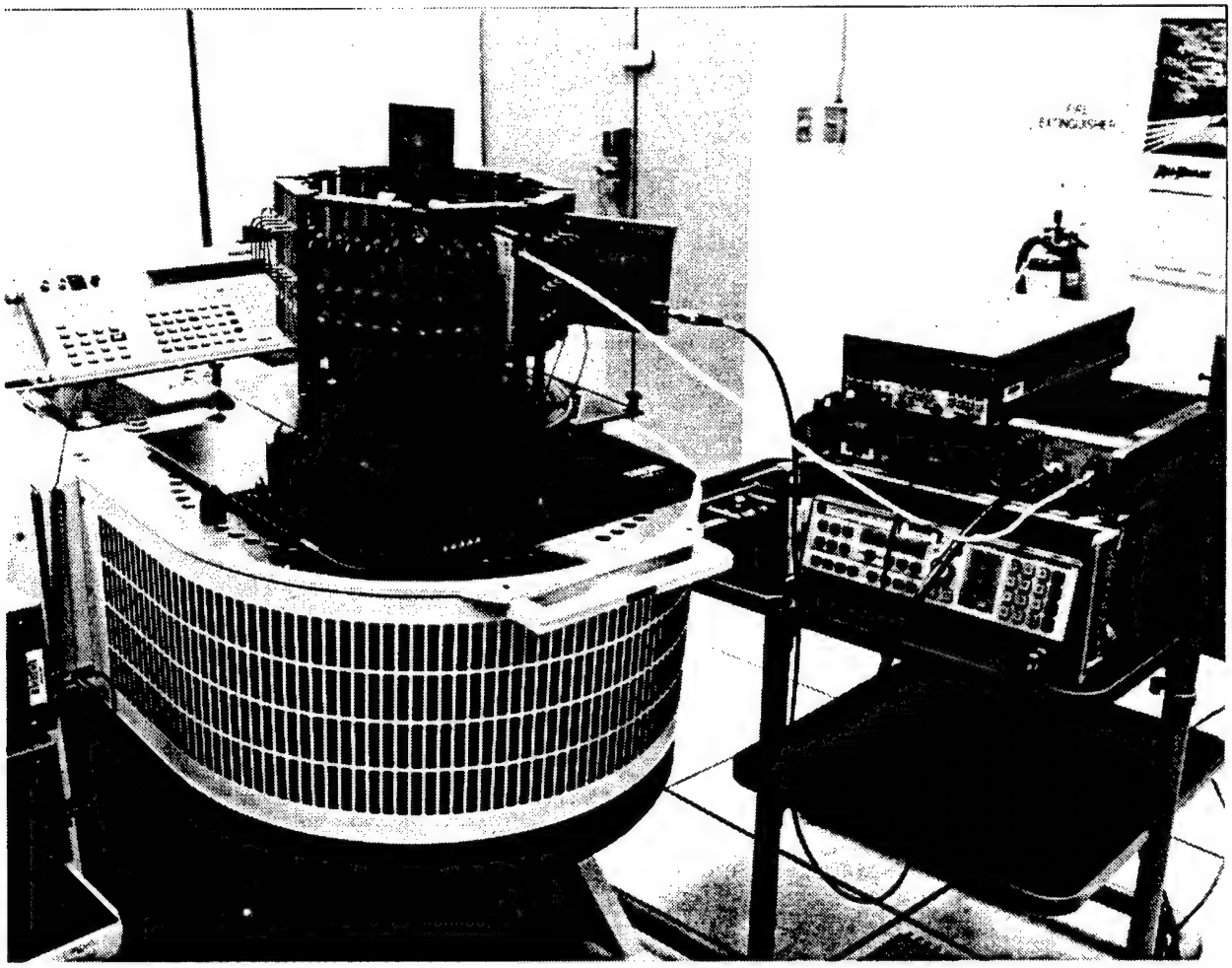


Figure 4.2-1: EMEAP Test Fixture in Test on the Advantech test head

a simple pattern that detects basic functional and interconnect problems. The Flash EPROM devices, due to long erase and write times, were tested with an erase-write-read sequence on 3 or 4 devices at a time, in two passes, using inverted data on the second pass. The test program data was encoded to enable identification of a failing device. The test frequency was 1.0 MHz for the SRAM and for EPROM read tests.

As a first step in testing the PMM in the EMEAP test fixture, the PMM was placed in the socket of the Advantech adapter board. The PMM test was run to make sure the test adapter is properly seated onto the test head and the PMM is properly seated in its socket. Then the PMM was removed from the socket, the EMEAP test fixture was placed on top of the Advantech test head and the modified Advantech test adapter board, and the test fixture was connected to the Advantech test adapter socket. One of the adapter sets described in paragraph 6.2 is used to adapt the PMM to the test fixture. The

PMM was plugged into the top of the test fixture, all of the through-signal adapters were attached to the test fixture, and the test program was run again. The test program was successful, and we did not have to reduce the clock speed of the PMM test, which was run at 1.0 MHz.

After the test program passed with the EMEAP test fixture in place, we selected a signal line to test. The line chosen was MPER13, PMM pin 33, which is a data line that goes to both static random access memory (SRAM) and the flash RAM. At 1 GHz the test passes at +30 dBm and fails at +31 dBm, so the susceptibility level would be +31 dBm. At 2 GHz the test passed with interfering signals as high as 2 watts (+33 dBm). We tested for susceptibility at a number of other frequencies between and 1 and 2 GHz and the frequency dependent susceptibility is plotted in Figure 4.2-2. Then we moved the diplexer to another data line, MD13, which is on package pin 49. The susceptibility of MD13, which is somewhat different from that of MPER13, is shown in Figure 4.2-3. This indicates that different circuits have different electrical characteristics, especially in terms of their susceptibility to interfering signals.

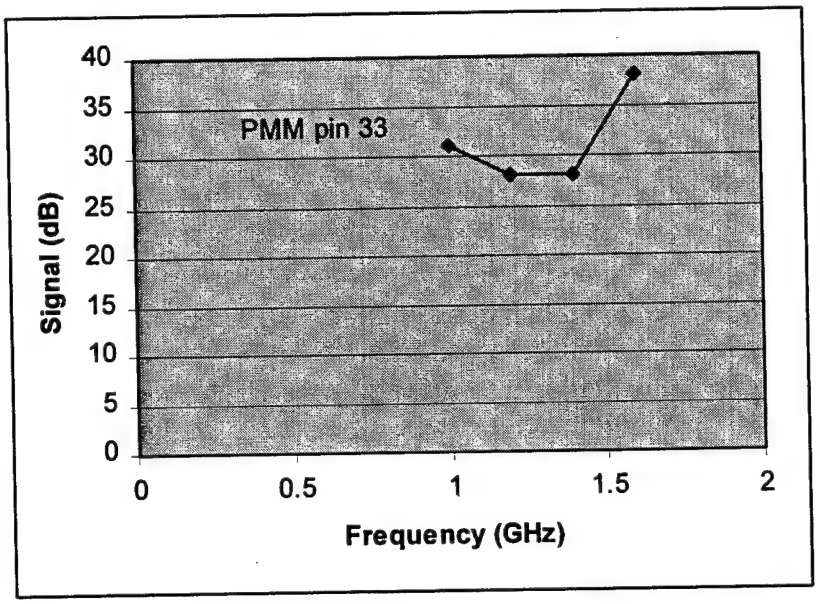


Figure 4.2-2: PMM Test Results, MPER13 (Pin33)

Once this initial testing was completed, we performed testing from 100 MHz to 7 GHz as we attempted to find the susceptibility points at a number of frequencies. This testing was performed on MPER13. The results are shown in Figure 4.2-4, and are displayed in dB across the frequency band from 100 MHz to 7 GHz. With 20 watts of output power we were not able to make the test fail at 2 GHz and above. This correlates roughly with the results of the modeling. The test data sheets from the PMM testing are shown in Appendix G.

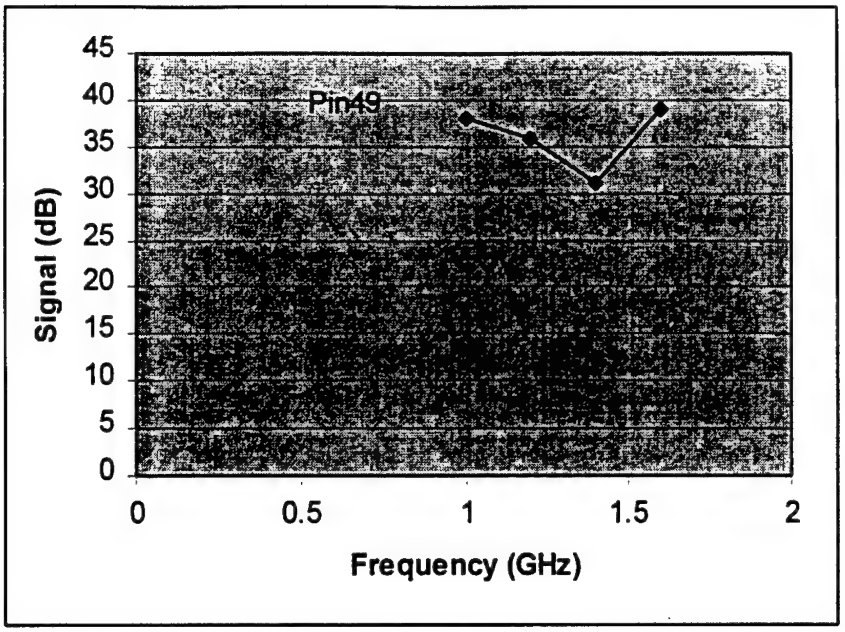


Figure 4.2-3: PMM Test Results, MD13 (Pin 49)

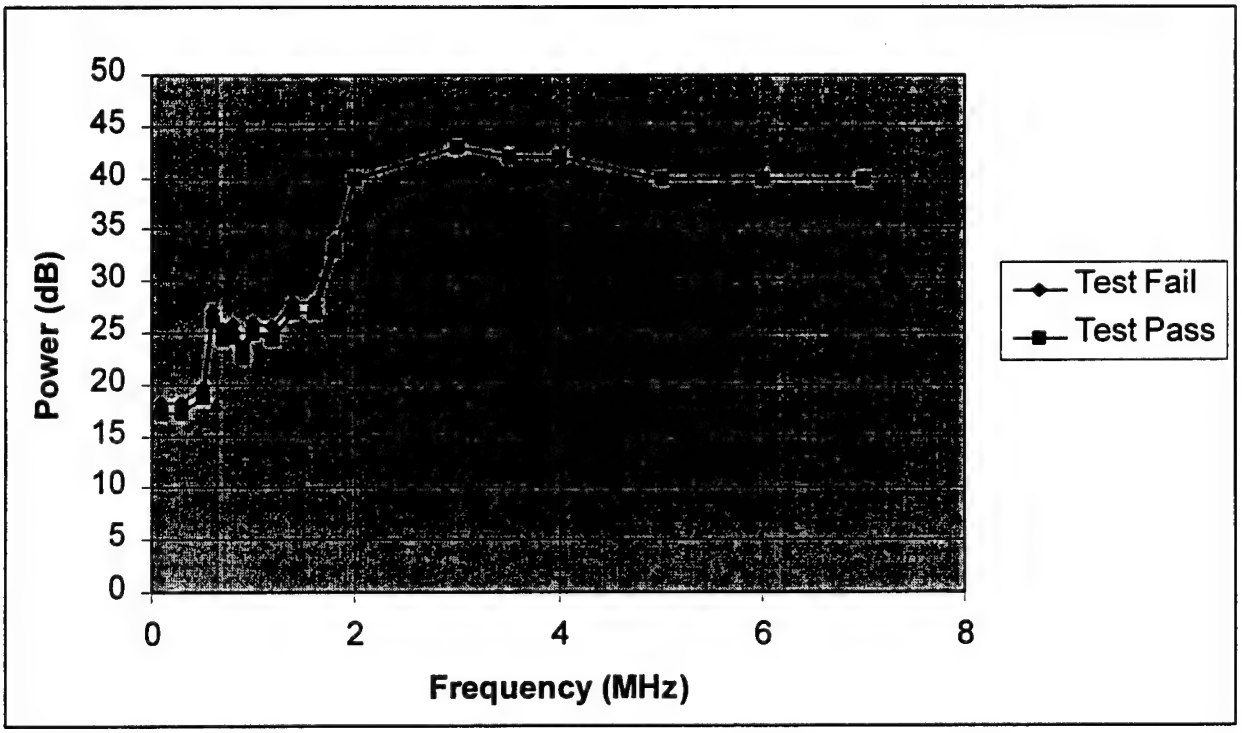


Figure 4.2-4: PMM Test Results, MPER13 (Pin 33)

4.3 Susceptibility Test Results

While performing the conducted susceptibility testing we were able to find susceptibility in both the 3DMM and the PMM to interfering signals at various frequencies and signal strength levels. Because there were simulation results for the 3DMM, we were able to compare the results of the simulation to the test results. Figure 3.2-3 shows that a simulated 1-volt signal will cause noise concerns at 550 MHz, just above 1.0 GHz, and at 5.5 GHz, on data line DQ3 of the 3DMM. There are also a number of areas above 1.5 GHz where a signal would have to be quite strong to interfere with operation of the device. A test was performed on the 3DMM at 100 MHz on the positive power supply line, Vcc, and we determined that a 1.2-volt signal on the power line would cause the test device to cease its normal operation. However, testing performed on data line DQ3 with a 100 MHz signal showed that the data line is much less susceptible to interference than was indicated in the simulation. We also performed two-signal sensitivity testing on the 3DMM and found interesting results for the test condition of a 1 GHz interfering signal being fed to a data line and a 1 MHz signal being fed to the power supply line. We found that if one interfering signal were very near its susceptibility threshold, a weak interfering signal applied to the other input would result in failure of the device to operate. We don't think that there is a simple linear relationship for the susceptibility of the two interfering signals, but there is definitely a relationship between two or more interfering signals and their susceptibility thresholds.

The simulation of the PMM did not proceed far enough to produce simulation data to compare with the test data, but through testing we found that the data inputs were sensitive to external RF energy. We tested two different data lines on the PMM over a wide range of frequencies and found that both were susceptible to the interfering signal, but they did behave differently. This indicates that there are different coupling factors between different pairs of adjacent lines or that the input gates react differently to externally applied interfering signals. An interesting design detail of the PMM is that the Vcc (DC power supply) line and the flash EPROM programming voltage line do not go through the PMM140 pin edge connector but are fed through an externally supplied wire. Because of this, we were not able to perform susceptibility testing on the PMM power lines.

5.0 DESIGN RECOMMENDATIONS

This section contains a list of recommendations for the design of advanced packaged devices. The recommendations were obtained, partially through observations made during the fulfillment of this contract, and partially through experience that has been accumulated in working with electromagnetic phenomena. These recommendations were not validated because it was not possible for us to have the test articles modified to determine if there was any change in performance.

In the process of writing these recommendations we also talked to a number of application specific integrated circuit (ASIC) and packaging designers and asked about their design process. We found that each designer seemed to have his own well-organized set of rules and procedures that they use in their design work. Several project groups use a proprietary high-speed electronic packaging

design handbook, but all the rules and guidelines found therein were obtained from the sources referenced in section 9 or through extrapolation of data in those sources. The designers also reference a number of design texts that have become de-facto design standards, and many of these appear in the references. In addition to these guidelines, each substrate manufacturer has their own set of rules that must be followed to ensure manufacturability and overall performance of the substrate. Many of these rules affect the electrical performance of their design and will help avoid EMC problems.

We also found that the microwave frequency designers have at their disposal many sophisticated design and analysis tools that were not available just a few years ago. Several of these tools are EESOF Libra, HP Microwave Design System (version 7), HP Advanced Design System, Cadence Spectre RF and Spectre HDL, Mentor Accusim, HP Momentum, and Sonnet EM. Included in these tools are layout libraries of standard shapes or parts, design and layout tools, circuit simulators, electromagnetic simulators, and field wave solvers. These tools will help the designer analyze and optimize the circuits as well as help them avoid potential EMC problems. In the packaging design stage many designs are analyzed using a three-dimensional circuit simulator. The use of these design tools is probably the biggest aid in proper design of advanced packaged devices, because the tool will help the designer find and eliminate problems with cross-talk, signal reflection, ground-bounce, and other RF circuit maladies that could lead to adverse EMC situations.

Following this paragraph is a list of additional recommendations to apply in the design of advanced packaged devices. Before applying the recommendations, the designer needs to determine if the circuit or system is in the high-speed region, where EMC related problems might surface. 8 MHz appears to be the dividing line between high speed and low speed digital systems. Digital devices typically used at or above this frequency tend to have fast transition times, and will require more careful attention to RF design that will those that operate below 8 MHz. High-speed conditions will also be present if the edge transition time of a device is faster than 2 times the propagation delay across the device. Analog or digital systems operated below this frequency will generally require less attention to design detail. Remember also that the bandwidth of a signal is not the clock frequency, but is approximately the 5^{th} harmonic of the signal. For typical high-speed digital devices, the signal rise-time = .07 X the clock period.

For high-speed systems, especially those to be designed using advanced packaging techniques, we would recommend the following:

1) Controlled impedance printed wiring boards must be used for all high-speed systems.
2) For controlled impedance printed wiring boards, hold the manufacturing tolerances of the finished board impedance to +/- 10% of the design values.
3) The maximum allowable length of an impedance discontinuity, including multiple short discontinuities, is 0.8".
4) Design circuit board so that traces will result in unloaded impedance levels of approximately 45 to 55 ohms for strip-line and dual strip-line layers and 55 to 80 ohms for microstrip and buried microstrip layers to keep in-plane crosstalk low.
5) Allocate the layer stack-up of a multi-level board with no more than 2 signal layers between reference planes.

6) Define layer stack-up to optimize return paths as well as signal isolation.
7) Use ground planes and power planes to minimize loop area for de-coupling.
8) Ground and power planes must remain continuous over their entire surface to prevent noise generation due to high impedance in the return path.
9) Separate return path planes may be necessary for mixed signal (analog/digital) printed wiring boards.
10) The length of a conducting line should be less than 1/10 wavelength of the highest frequency component of the signal.
11) Limit crosstalk to 5% of Vcc or 50% of the noise margin through proper design.
12) Signal lines, especially clock signals, need to be properly terminated to eliminate reflections.
13) Use series termination wherever possible (except for bipolar devices) for simplicity and reduced power consumption.
14) Locate series termination as close as possible to the output pin of the device which drives the net (0.8 inches for 1 ns designs).
15) Locate the load termination so that the terminator is the last device on the net.
16) De-couple all active devices through the use of low ESL surface mounted capacitors that are no more than 0.1" away from the power pin.
17) Size the de-coupling capacitors based on transient current required during simultaneous switching of the semiconductor devices.
18) Routing of adjacent signal layers must be orthogonal to eliminate broadside cross-talk.
19) Route all critical nets in equivalent impedance layer pairs to reduce mis-matches.
20) Route all nets by shortest possible means without resorting to branching.
21) Route data and address busses on signal layers that are on opposing sides of reference planes.
22) Critical nets should traverse no more than two layers.
23) The maximum number of vias (not including component lead vias) between two component leads is two.
24) Allow at least one ground pin, symmetrically spaced, for every eight signal pins for board-to-board connectors
25) Each power pin in a connector should have a ground pin immediately adjacent to it to reduce inductive loop area.
26) If high isolation must be maintained through a connector without using coaxial cable, signals should be surrounded on four sides by reference pins.
27) Liberal assignment of ground pins throughout connectors will reduce high frequency loop area as well as provide some shielding against RF radiation and susceptibility.
28) All clock signals pass through a board-to-board connector should be guarded on each side by ground or power pins.

6.0 TEST FIXTURE DEVELOPMENT

This section describes the design, fabrication, and acceptance testing of the conducted mode test fixture, which was developed as part of this contract. Development of the signal combiners, which are used in conjunction with the test fixture, is described in section 7.0. The test concept was developed for a conducted interference test fixture that would be able to test, as a minimum, the 3-D memory module (3DMM) and the processor memory module (PMM). But the test fixture that was developed had other features that would make it suitable, with some adaptation, to test a number of advanced technology devices. Test fixture development includes design, fabrication, and acceptance test of the test fixture.

The initial development of the test fixture was focused on the 3DMM and a fully functional version of the PMM. The 3DMM package has 50 pins, and only one of those pins is not connected to a signal or power/ground line. The test interface to the PMM was through an 80-pin interface. However, when development of the full PMM was suspended, we found that access to the memory portion of the PMM was through a 140-pin "edge-board" connector, of which 119 were signal, power, or ground lines. In short, we needed to design a test fixture that would accommodate approximately 120 signals, either directly through the test fixture or through test adapter bypass circuits.

We were not able to find a single purpose combiner that was able to support conducted interference tests over a very wide frequency range and at high RF power levels. Therefore, we decided upon a plug-in signal interface that would allow different signal combiners to be used with the test fixture. After performing a number of trade studies an octagonal test fixture, with 40 signals that pass directly through it, was selected. Different test adapters with signal bypasses and a method to bypass the main test fixture make it possible to test the 50 pin 3DMM and the 140 pin PMM. The development of these signal combiners is given in section 4.0.

We chose an automated tester as our instrumentation baseline in order to adequately characterize devices of the complexity of the PMM and 3DMM. Our test fixture and the signal combiners perform the function of a test break-out unit, located between the automatic tester and the test device, which will allow us to insert interfering RF signals into the signal, power, or ground traces of the device under test.

6.1 Test Fixture Concept Development

Based upon the connector interface of the two parts we have chosen for the test program, we began several different test fixture configurations to determine the optimum layout. The block diagram of the test fixture is shown in Figure 6.1-1, and it shows the major elements of the tester, including signal routing. The first test fixture concept that was pursued was a single board flat fixture with a physical layout similar to that shown in Figure 6.1-2. The device under test plugs into a socket in one end of the fixture, the umbilical from the automatic tester plugs into the other, and plug-in signal combiners would be plugged into sockets on both the top and bottom sides of the fixture. Because the plug-in signal combiners were to be arranged in a matrix layout, the RF signal traces from the lower combiners to the test device might be as much as 8" longer than the traces from the top row of

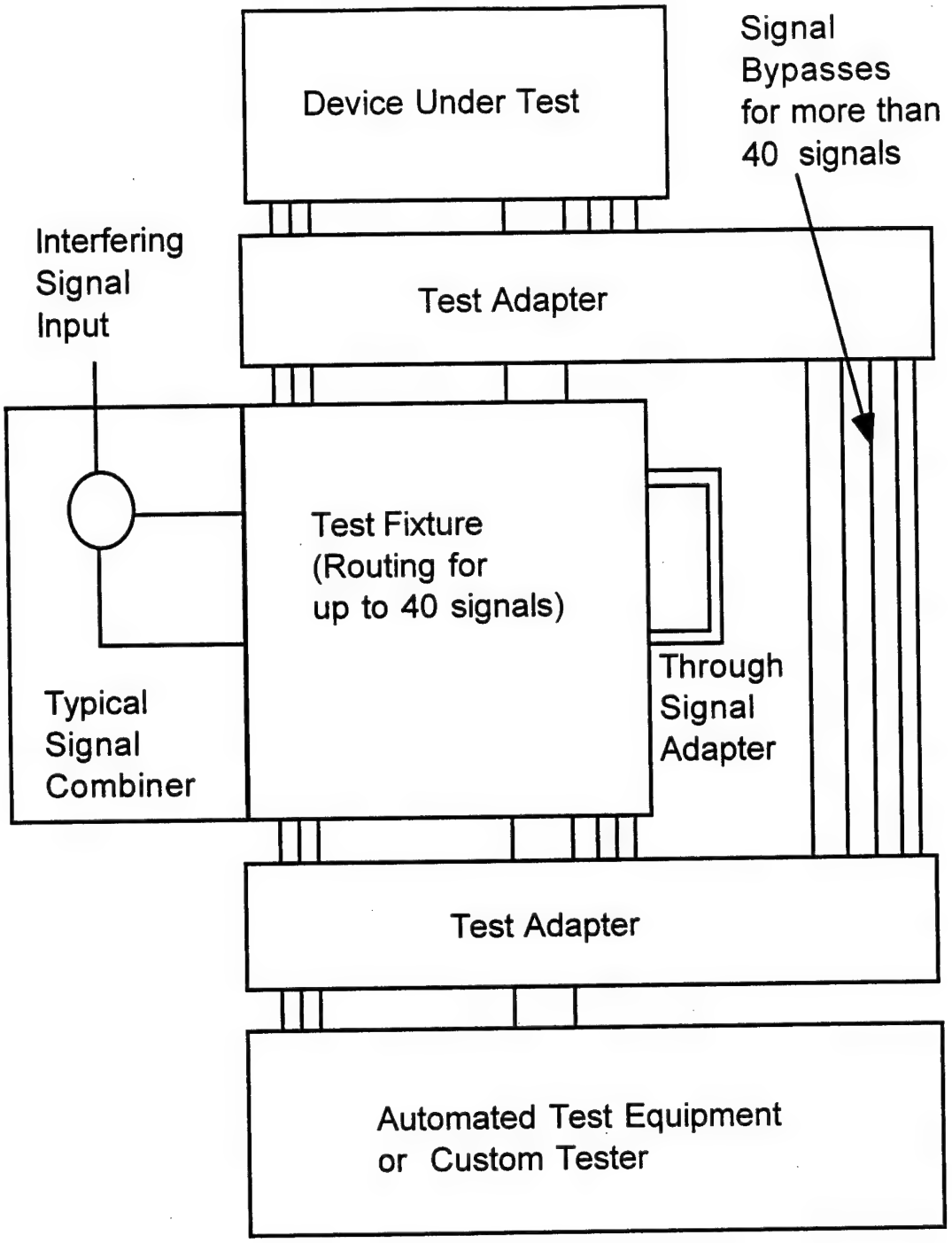


Figure 6.1-1: Block Diagram of the Test Fixture

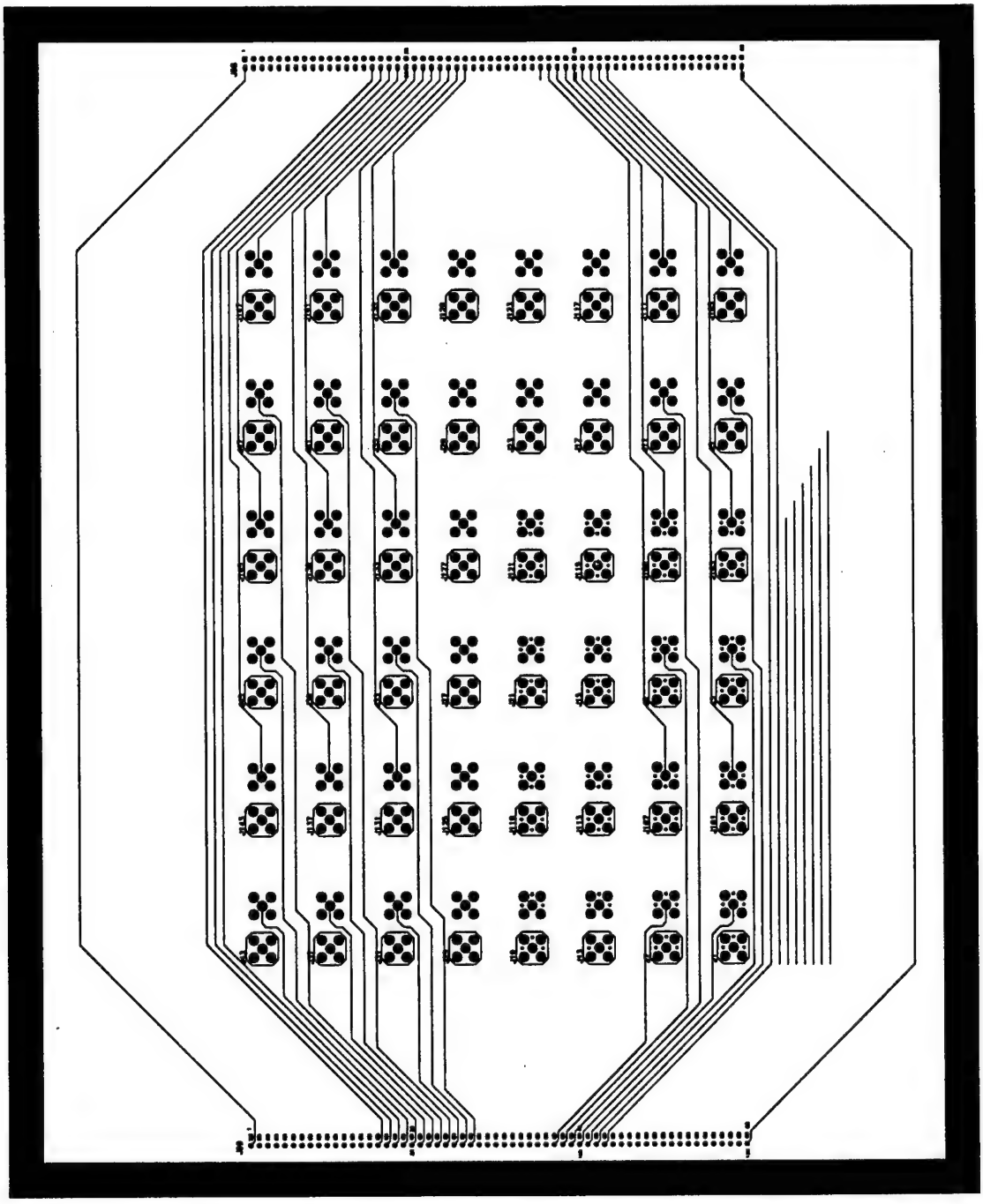


Figure 6.1-2: First test fixture concept - flat fixture

combiners. This would cause unequal RF losses between the various signals and it would be difficult to determine true RF susceptibility levels.

Because of the poor RF performance of the flat fixture we determined that a cylindrical fixture, with connector pairs on the edges of the cylinder for insertion of plug-in signal combiners, would give better performance. An isometric view of this fixture concept is shown in Figure 6.1-3 and a cross section view, which also shows the interface to a typical signal combiner, is shown in Figure 6.1-4. The size of this fixture was a concern to us because as the number of signals increased, the size of the fixture and the length of the individual signal lines would increase. If the width of the signal combiners and hence the spacing between the signal traces could be reduced, then the size of the fixture could be reduced for the same number of signals.

6.2 Test Fixture Detail Design

Once the basic concept for test fixture was established, detail design was started. The top and bottom circuit boards for the test fixture are similar to each other, although there are fundamental differences between them. Both boards needed to be identically the same shape and the connector locations needed to match so that the signal combiners would mate vertically between both boards. The boards are different in that the top board is required to carry combined digital and RF signals and the bottom board is only required to carry digital signals.

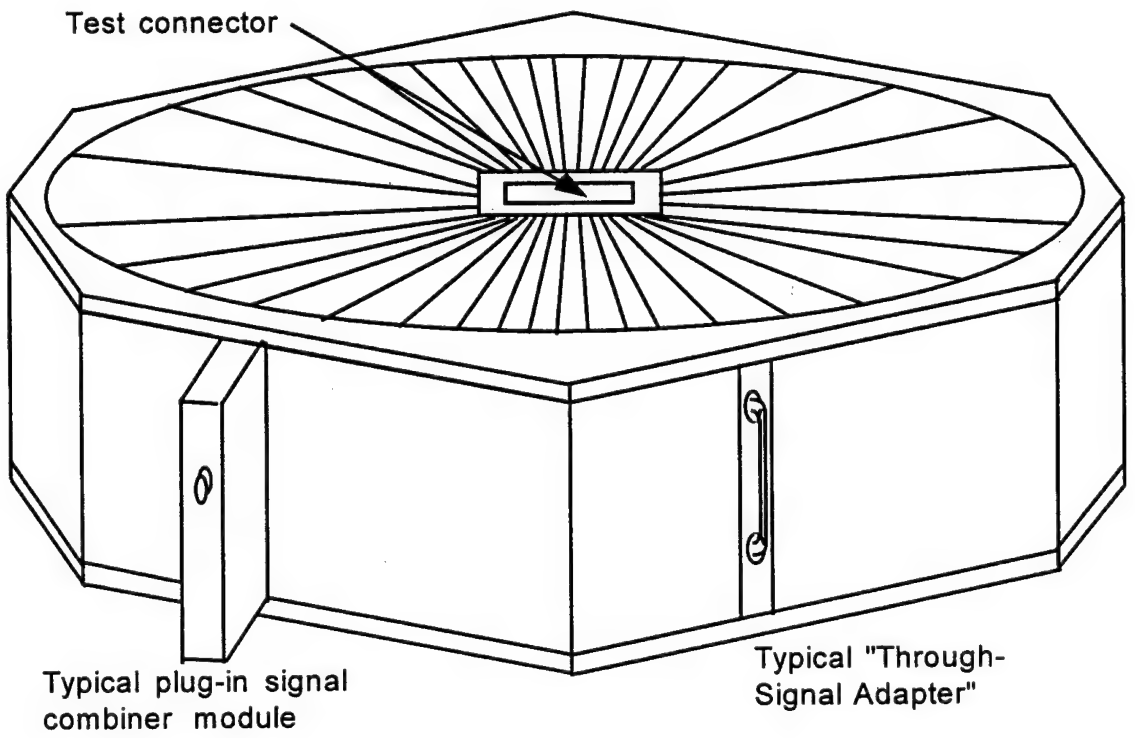


Figure 6.1-3: Test Fixture Concept – Cylindrical Fixture

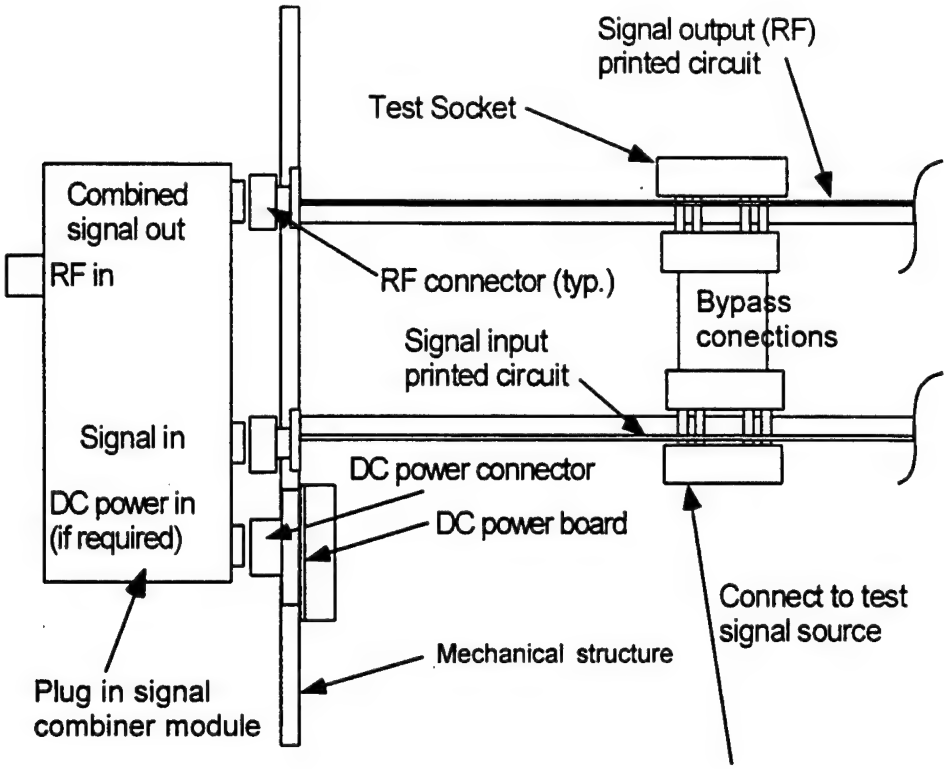


Figure 6.1-4: Test fixture cross section view

The first detail to be worked out was the size of the test fixture circuit board and the spacing between the signal combiners, which required that the detail design of the signal combiners had to proceed concurrently with that of the test fixture. The high power op-amp signal combiner and the wide-band amplifier/diplexer combiners ended up being the thickest. When detail mechanical design was complete, these combiners were approximately 0.75" thick. We allowed for a little space between plug-in modules and chose 0.80" module to module spacing. With the module to module spacing and number of total plug-in modules established, we began some preliminary layouts. A totally round test fixture would have been nice from the standpoint of equal length signal lines and symmetrical board layout of the top and bottom test fixture boards, but it made the test fixture to signal combiner mechanical interface too difficult. We looked at square, hexagonal, and octagonal shapes for the basic test fixture, and the octagon was the clear choice. Then we tried layouts with 5 modules per edge versus 4 or 6 modules per edge, and finally settled on 5 modules per edge. The final printed circuit layout for the bottom board is shown in Figure 3.2-1. The size of the printed circuit layout for this design was approximately 12" X 12" without connectors or signal combiners.

The top board of the test fixture is required to carry high frequency digital and RF signals. Rogers TMM-3, a low-loss microwave laminate with a dielectric constant of 3.27 and a material thickness of 0.020", was chosen for the material so the losses at high frequency would be minimal. The RF signals from the external interfering signal source and the digital signals from the Advantech tester are matched to 50 Ohms, and the input lines from the signal combiners were designed as 50 ohm

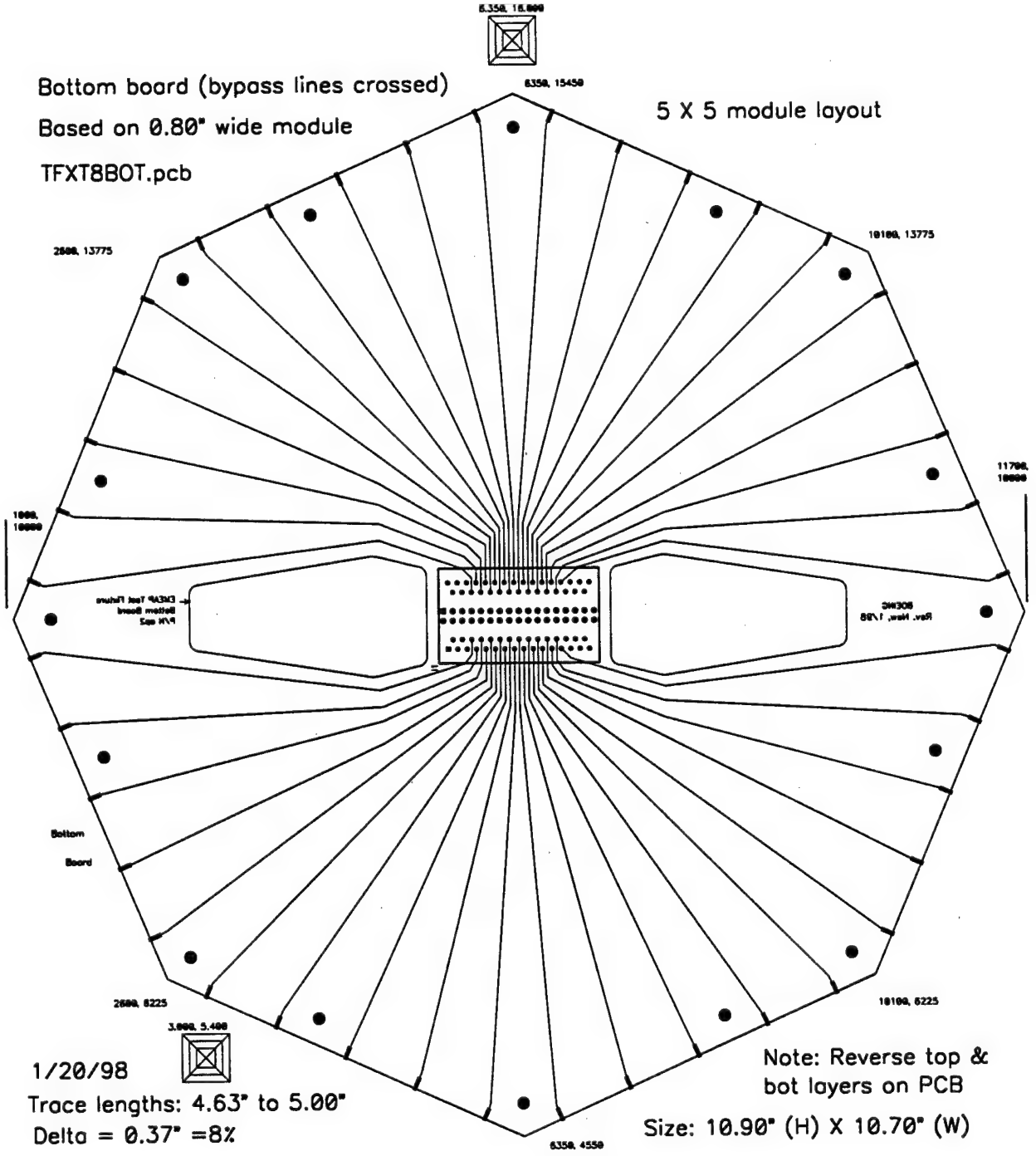


Figure 6.2-1: Printed Circuit Layout – Bottom Board

transmission lines, which for .020" thick Rogers TMM-3, are about 0.050" wide. Because the impedance of the device under test is, in most cases, much higher than 50 ohms, an impedance transformer was designed into each of the traces on the board to attempt to match the higher impedance of the test device. The choice of microwave material and thickness determined the impedance at the test socket end of the transition. The smallest practical line width line width is 0.010" and its impedance is about 110 ohms. One hundred ten ohms is lower than the impedance of most of the circuits that will be attached to the test fixture, so there will be an impedance mis-match at the test device. But it does provide a signal line with an intermediate impedance that will cause less reflection from the test device than would a continuous 50-ohm line. A section of the impedance transformer (notice the tapered lines) is shown at 200% of full size in Figure 6.2-2. The layout of the top board is shown in Figure 6.2-3. Although the electrical characteristics of the Rogers TMM-3 were very good, the material is very brittle, which requires it to be laminated to a layer of FR-4 fiberglass laminate so that it would withstand the stresses associated with inserting and removing the test articles and signal combiners.

During the development of the test fixture we were also working with various designs to adapt the 40-signal test fixture to test devices with up to 120 signal lines. This was done through the use of test adapters and signal bypasses, but it was done differently for the 3DMM than for the PMM. The basic test fixture was designed to accommodate the 3DMM, which utilizes a 50 pin quad-in-line socket. We were able to feed the 50 3DMM signals through a 40 signal test fixture, but not all at once. This was done by widening the 3DMM socket to 62 pins and creating bypass zones of 10 connections on the left and 12 connections on the right for the connections which fall outside the 40 pin interconnect area. This concept is shown in Figure 6.2-4. When the 3DMM is located so that pins 1 and 50 were at the left edge of the test connector, pins 1 through 5 and 46 through 50 bypass the test fixture through a ribbon cable and pins 6 through 45 pass through the test fixture. When the 3DMM is moved all the way to the right so that pins 25 and 26 are at the right edge of the connector, the signals on pins 20 through 31 bypass the test fixture through a ribbon cable and the signals on pins 1 through 19 and 32 through 50 pass through the test fixture. By designating two locations for the 3DMM in the 62-pin test socket, all 50 signals can be routed through the test fixture to test for susceptibility levels.

Finding a way to feed the 120 signals from the "smart card" PMM through the 40-signal test fixture provided a greater challenge than did the 3DMM. In order to test the PMM, we designed three sets of test adapters that would plug into the middle 40 pins of the 62-pin test socket. We divided the 120 signals into three groups of 40, and designed a set of test adapters for each group of 40 signals. Each pair of test adapters would route 40 signals through the test fixture and bypass 80 signals around the test fixture. The need to bypass so many signals led to the design of the test fixture with slots cut out next to the test connector. These bypass signals use different bypass connections than used by the 3DMM. This test adapter concept is shown in Figure 6.2-5. The top circuit and silkscreen layers of the three top adapters are shown in Figures 6.2-6, 6.2-7, and 6.2-8 at full size. The bottom adapters, which are not shown, are very similar to the corresponding top adapter. By selecting the appropriate test adapter set, each of the signals from the automated tester to the PMM, except for VCC and the Flash EPROM programming voltage, can be made to pass through the test fixture for susceptibility testing.

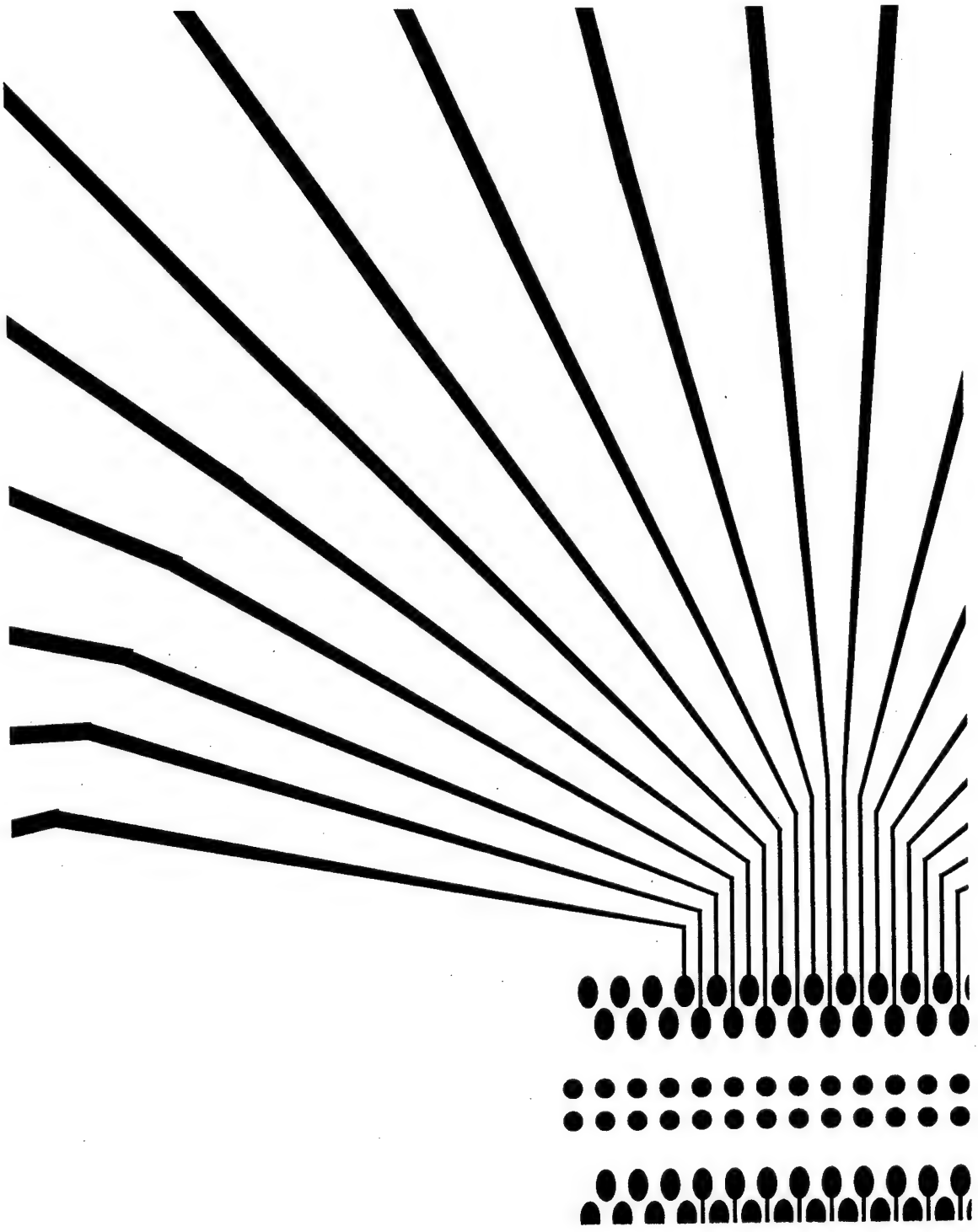


Figure 6.2-2: Microstrip Impedance Transformer

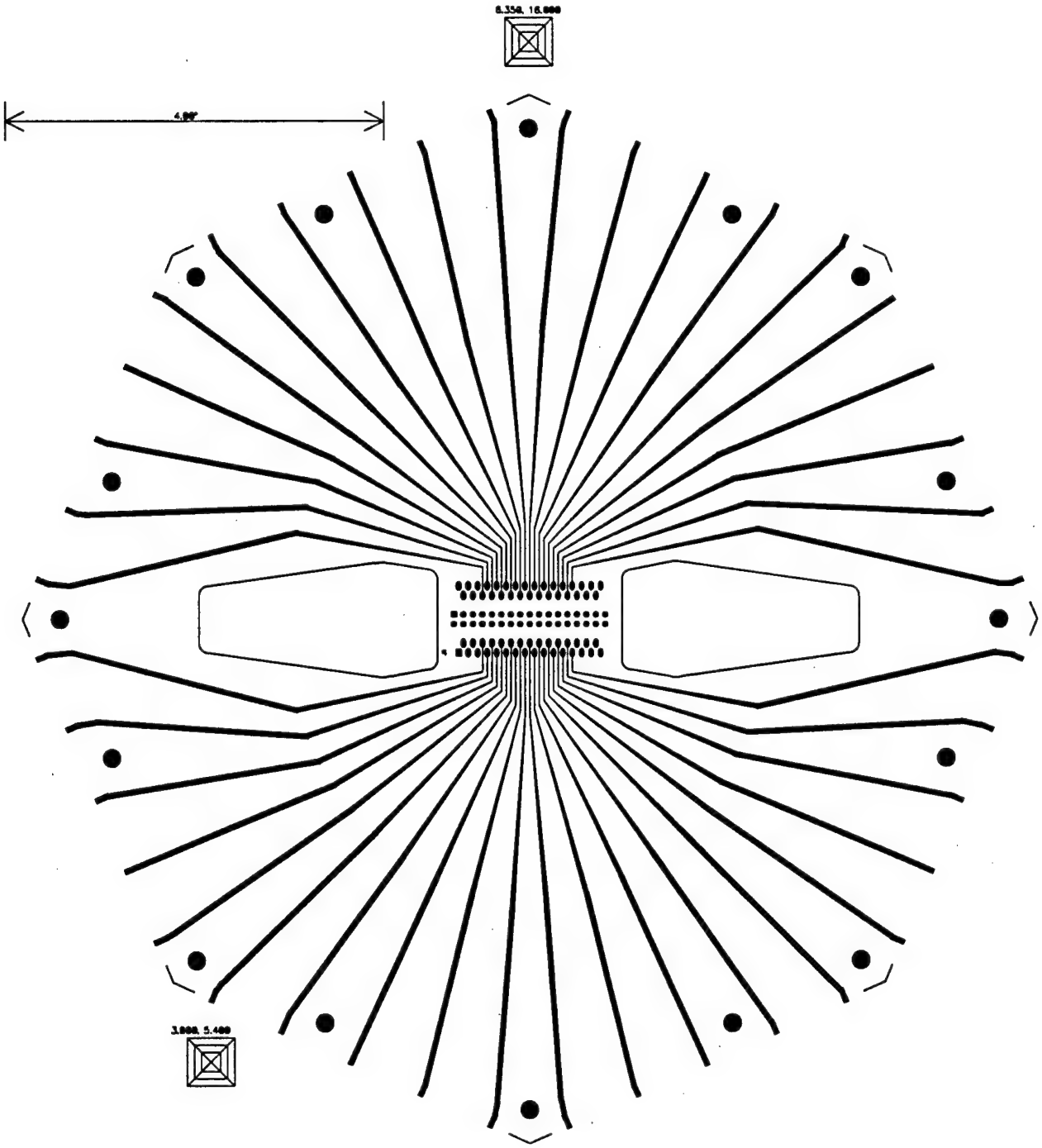


Figure 6.2-3: Top Printed Circuit Board

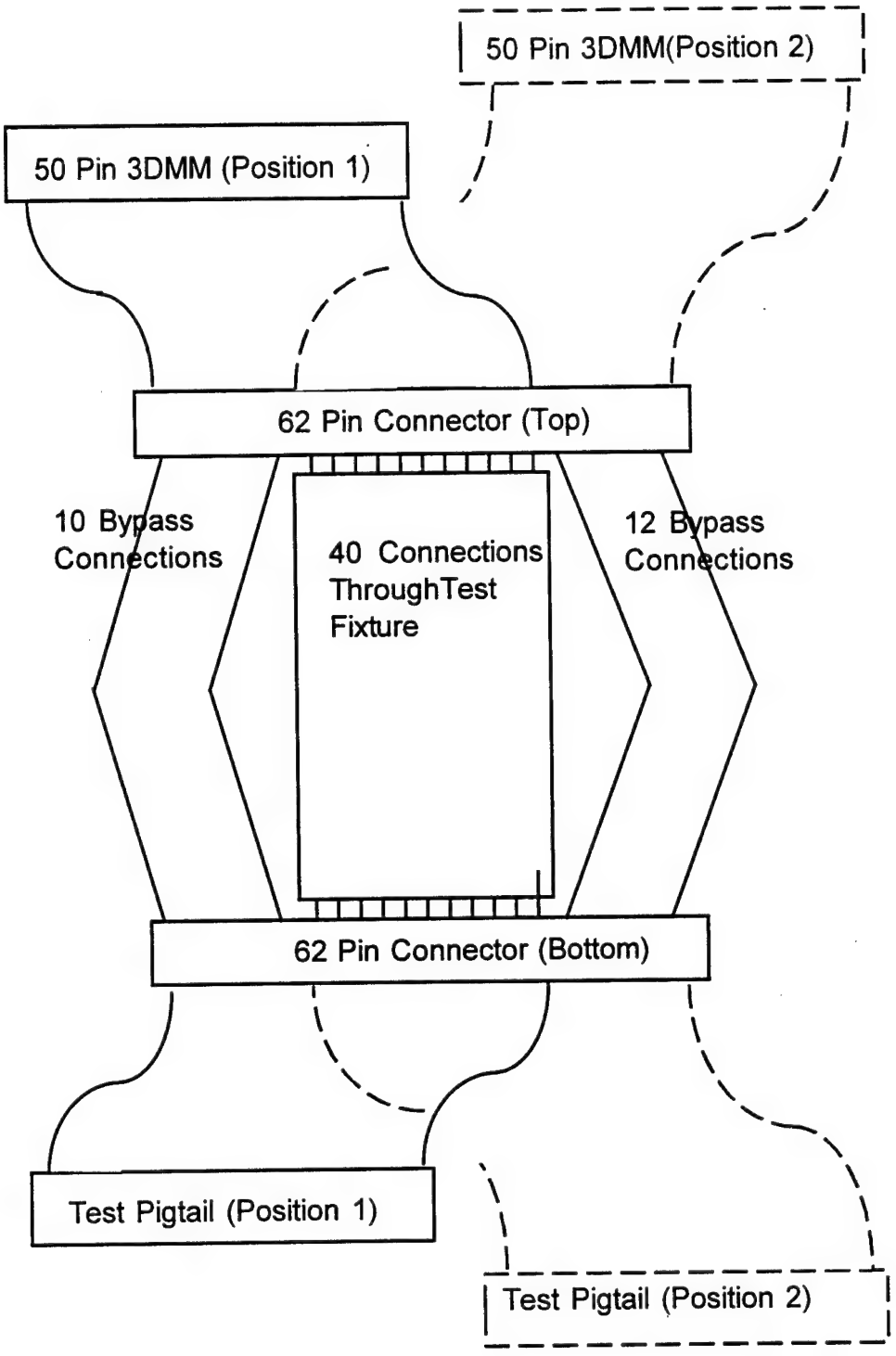


Figure 6.2-4: Concept to adapt 3DMM to 40 pin Test Fixture

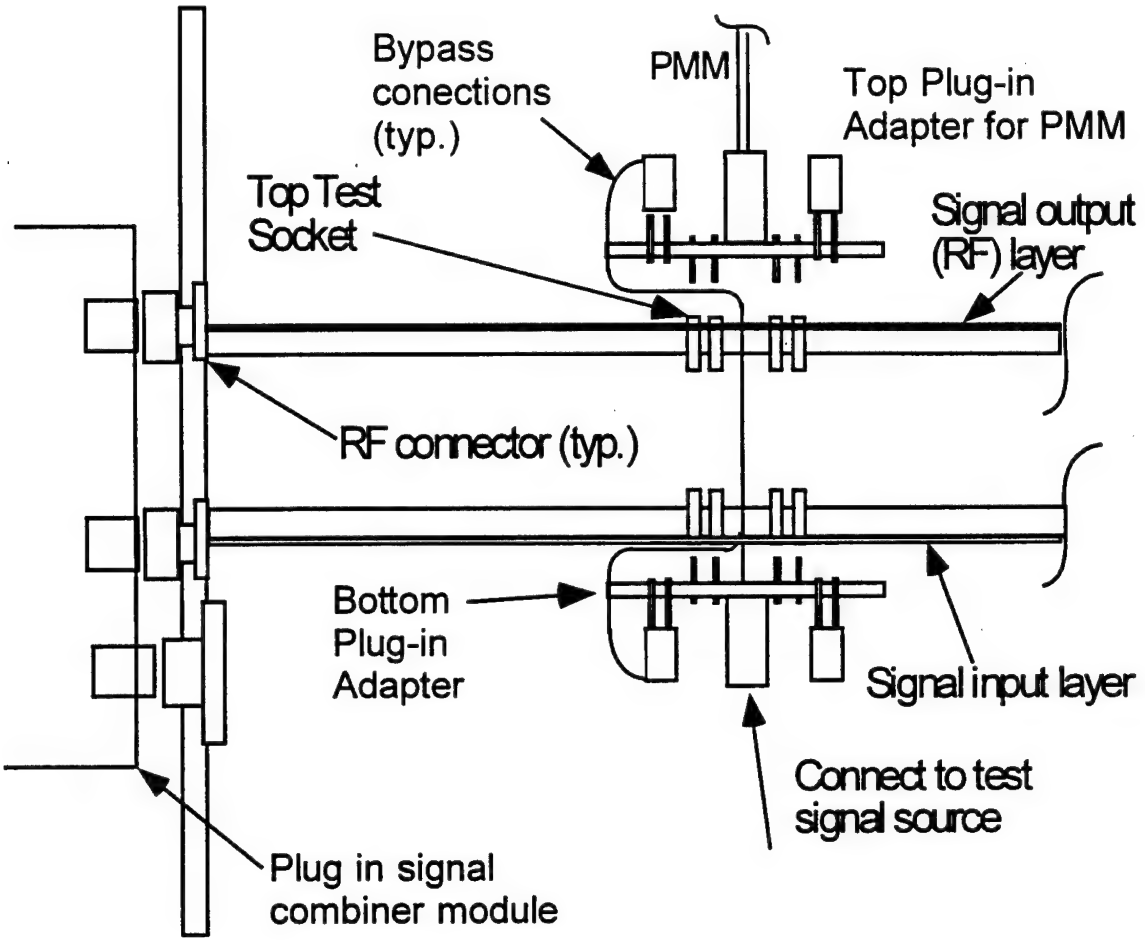


Figure 6.2-5: Test Adapter Concept for PMM Test

Once the electrical layouts of the two boards were completed, detail mechanical design was started. The test fixture boards are large enough that they needed to be fully supported in order to meet the tight dimensional tolerances between the input and output signal combiner connectors. The Rogers TMM-3 is also brittle enough that good support was necessary to prevent the board from breaking when the test devices or one of the adapters was inserted or removed. High quality RF connectors were also required to make the connection between the signal combiners and the test fixture boards. We chose to laminate the .020" thick microwave board to a .047" thick fiberglass laminate board to increase it's strength and resistance to breakage. We also chose to mount each circuit board to a 0.25" thick aluminum panel, which is machined to the exact shape of the board. The mechanical layout of the top and bottom platforms is shown at 55% of full size in Figure 6.2-9. The platforms are held in accurate vertical alignment by 16 bars, two on each flat edge of the 8 sides of the panels. These 16 bars form the major vertical structural members of the test fixture, and they also support the power boards

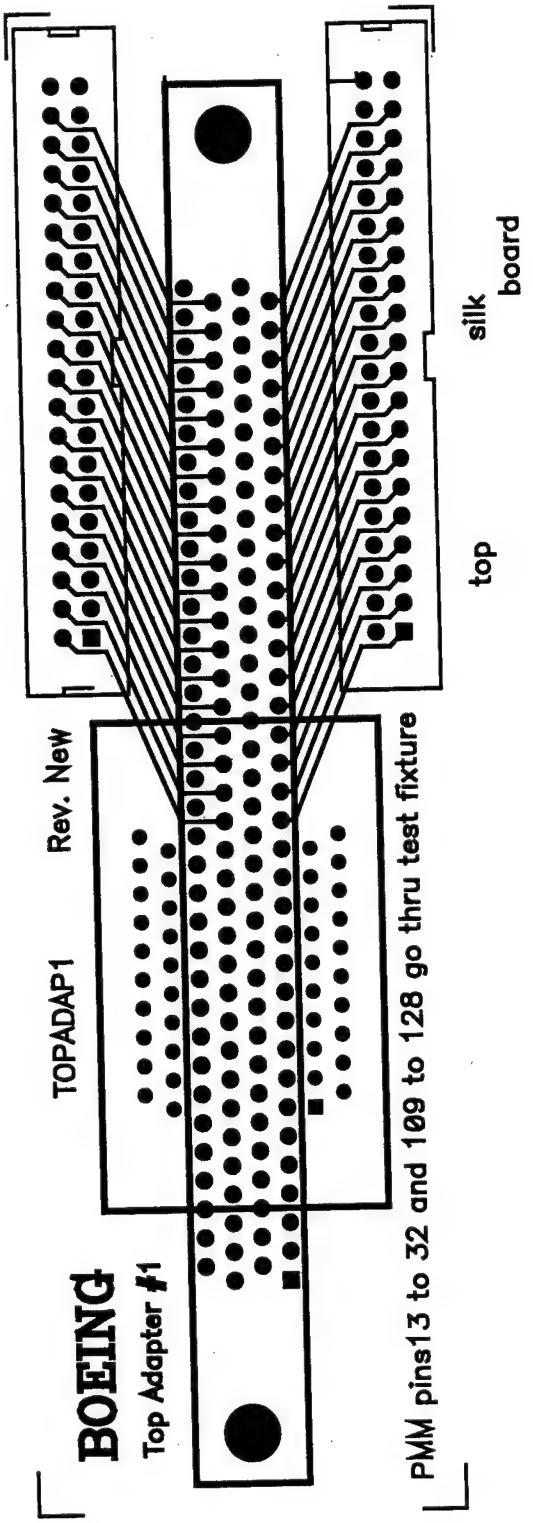


Figure 6.2-6: PMM Top Adapter #1

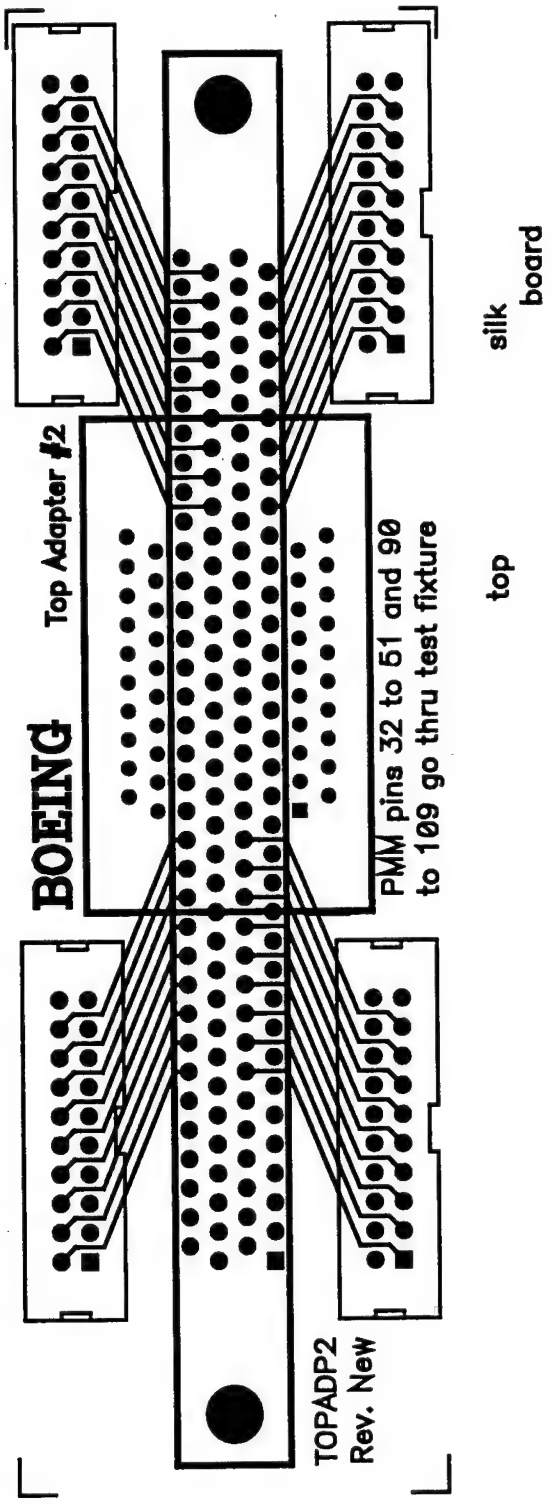


Figure 6.2-7: PMM Top Adapter #2

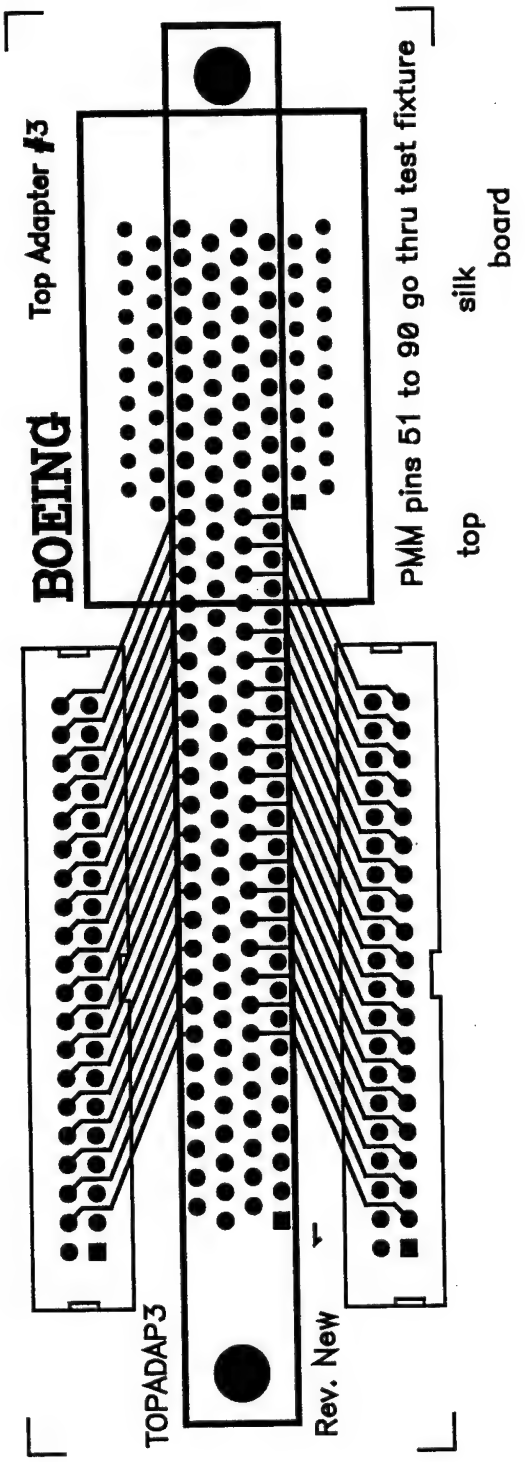


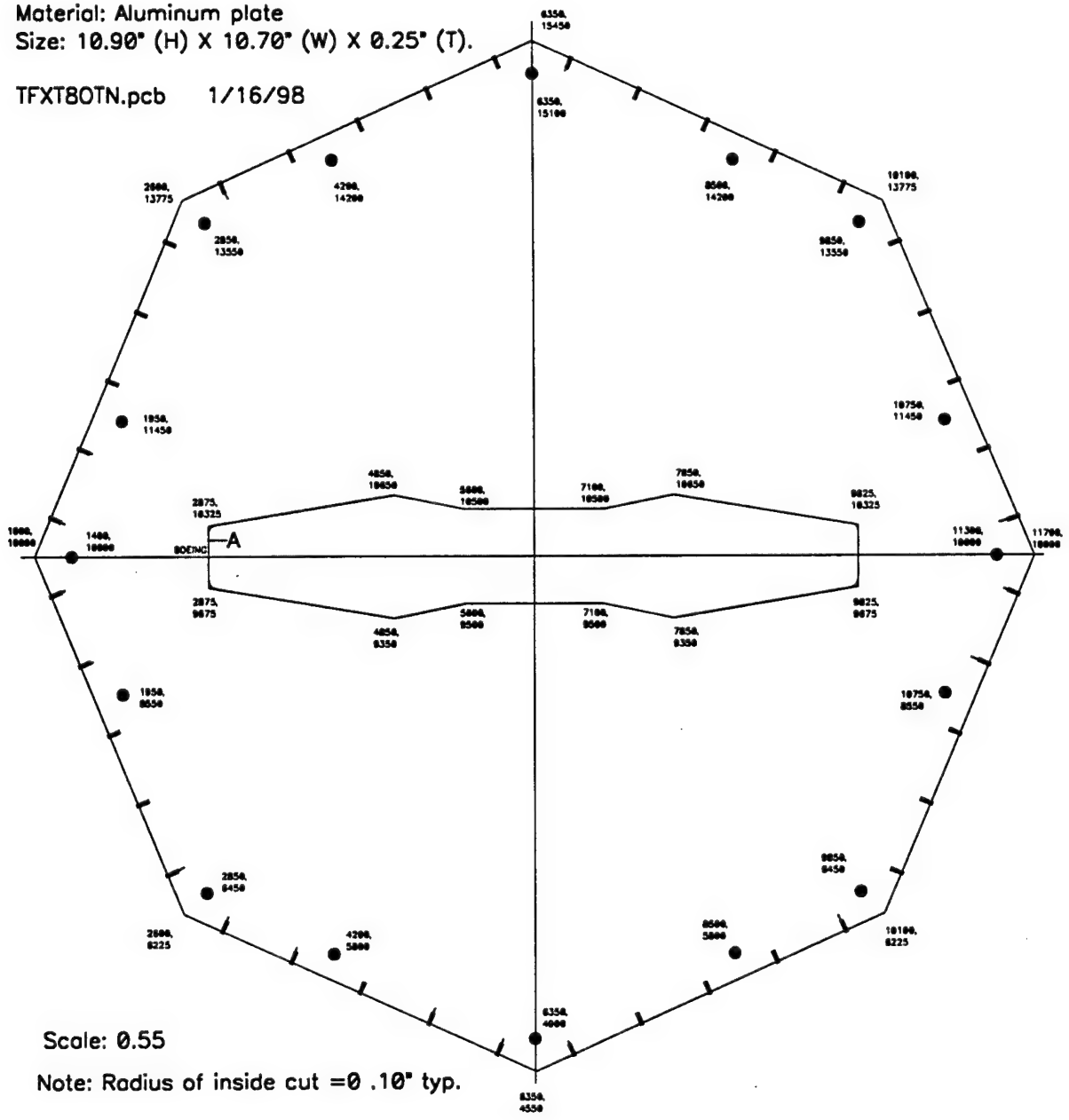
Figure 6.2-8: PMM Top Adapter #3

Top platform, pn apm1: Drill & tap #4–40, 16 Pl, (through) at locations shown.
Bottom platform, pn apm2: Drill & tap #4–40, 16 Pl, (through) at locations shown.
Dril l& tap #2–56 X 1/4 (min) deep, 80 Pl. around edge as shown in dwg. mechdes3.6.
Drill & tap #4–40 X 3/8 (min) deep, 16 Pl. around edge as shown in dwg. mechdes3.6.

Mark top platform "top" on top side.
Mark bottom platform "bot" on bottom side.
Cut a notch at point "A" to match platforms

Material: Aluminum plate
Size: 10.90" (H) X 10.70" (W) X 0.25" (T).

TFXT8OTN.pcb 1/16/98



Scale: 0.55

Note: Radius of inside cut =0 .10" typ.

Figure 6.2-9: Mechanical Layout of Test Fixture Platform

and the bars where the signal combiners are attached.

We chose to attach signal combiners to the edges of the test fixture as plug-in modules. This concept utilizes two pair of slip-on RF connectors as part of the mechanical and electrical interface. We could not find a slip-on connector that met all of our mechanical and electrical requirements, so we used an SMA (threaded) connector with a SMA to push-on adapter. The SMA connector is a 4-hole flange mount device made by Southwest Microwave and the SMA-to-OSP adapter is made by MaCom. The SMA connector is designed for operation up to 27 GHz, and it has a pin/socket interface to mount tothe edge of a printed circuit panel. The pin that connects to the printed circuit is only 0.005" thick. It is soldered to the top of the 50-ohm line, and because it is so thin, it launches the signal into the back of the connector with minimal disturbance of the voltage standing wave ratio (VSWR). The edges of each platform are drilled and tapped so the 16 vertical supports and 40 RF connectors can be attached to the platform with screws.

Several of the signal combiners require DC power for their operation. In order to provide DC power through a plug-in interface, DC power printed circuit board assemblies were added to the test fixture. The DC power boards have DC power receptacles that are bussed together with power traces. The boards are mounted just below the lower RF connector, and they are all connected to banana jacks that come to a panel on the side of the test fixture. Each signal combiner that requires DC power has a power plug that will mate with the receptacle on the DC power board. The printed circuit layout of the DC power board is shown in Figure 6.2-10 at 150% of full size. A drawing one of the sides of the test fixture is shown in Figure 6.2-11, and a picture of the completed test fixture is shown in Figure 6.2-12.

7.0 SIGNAL COMBINER DEVELOPMENT

In order to carry out the test program it is necessary to provide the capability to test the advanced packaged devices' susceptibility to interfering signals from about 10 Hz to about 18 GHz. This wide frequency range will cover signals ranging from AC power supply up through their operating frequency range and to include any credible interfering signal the test devices might see in it's operational environment. The signal combiners developed as part of the contract combine the digital signals at the device under test with an interfering signal in the frequency range of just above DC to 18 GHz. Semiconductor combiners were designed to cover the frequency range of about 10 Hz to about 150 MHz. Diplexer combiners cover the frequency range up to approximately 18 GHz. The layout chosen for the test fixture requires that either a signal combiner or a through signal adapter be inserted in each signal path of the test fixture in order to conduct the test signal from the bottom input layer of the test fixture to the top or output layer. The photograph in Figure 7.0-1 shows five through signal adapters mounted to the test fixture.

7.1 Signal Combiner Concept Development

The operating frequency range served by the test fixture is so wide that several different types of signal combiners were designed to cover the whole frequency range. We also needed to add

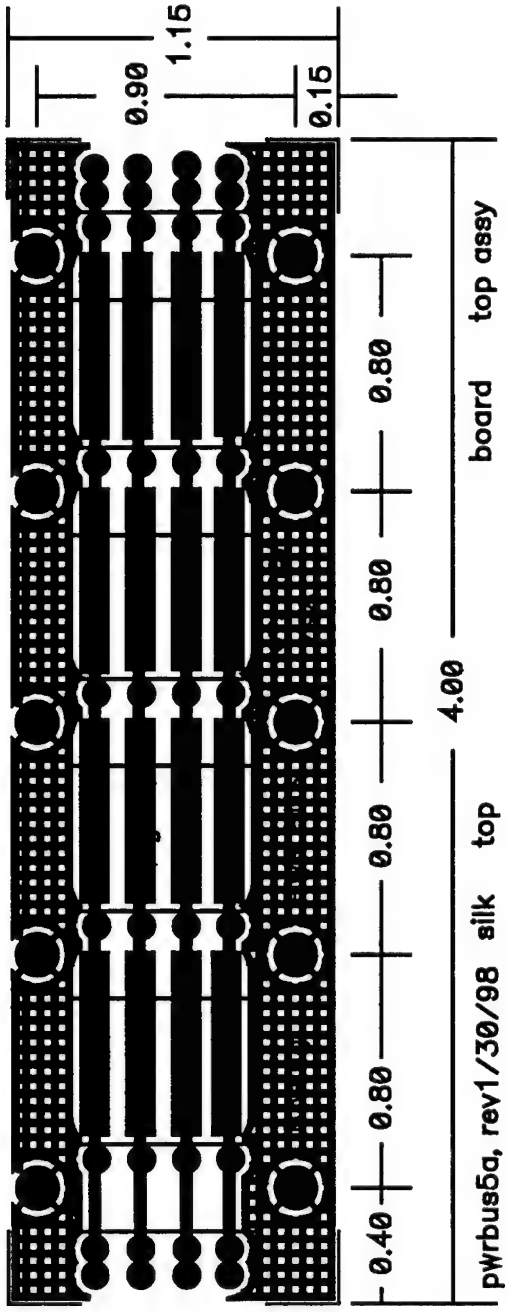


Figure 6.2-10: Printed Circuit Layout of DC Power Board

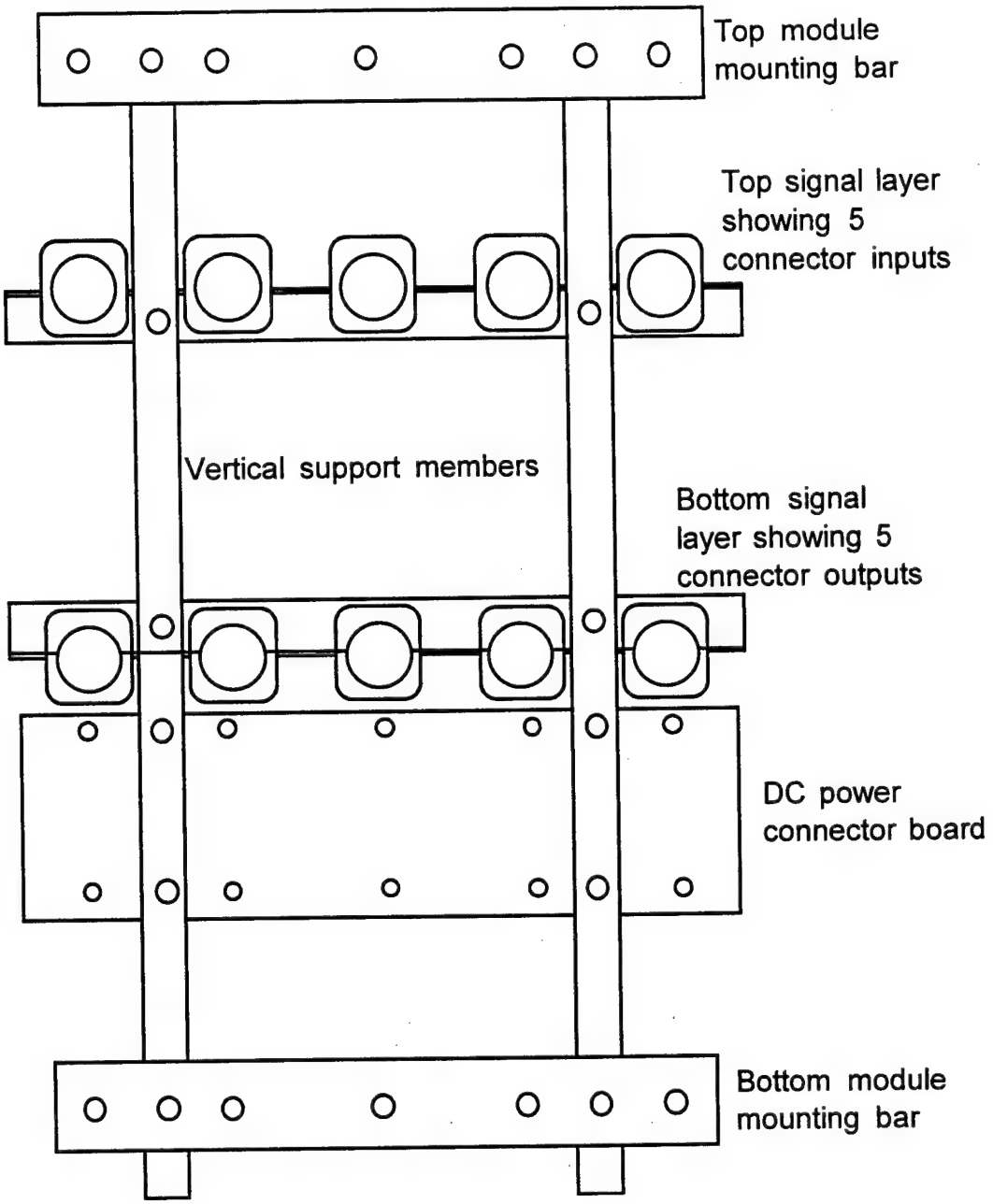


Figure 6.2-11: Side Detail of Test Fixture

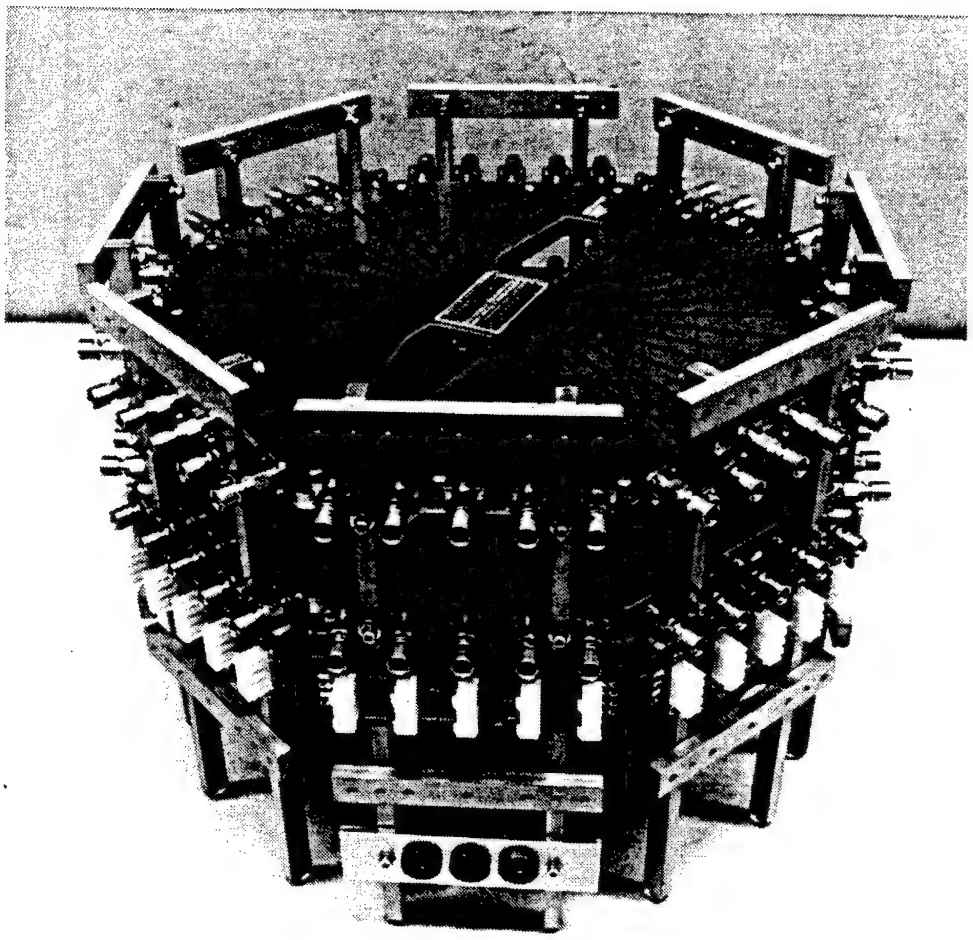


Figure 6.2-12: Picture of Test Fixture

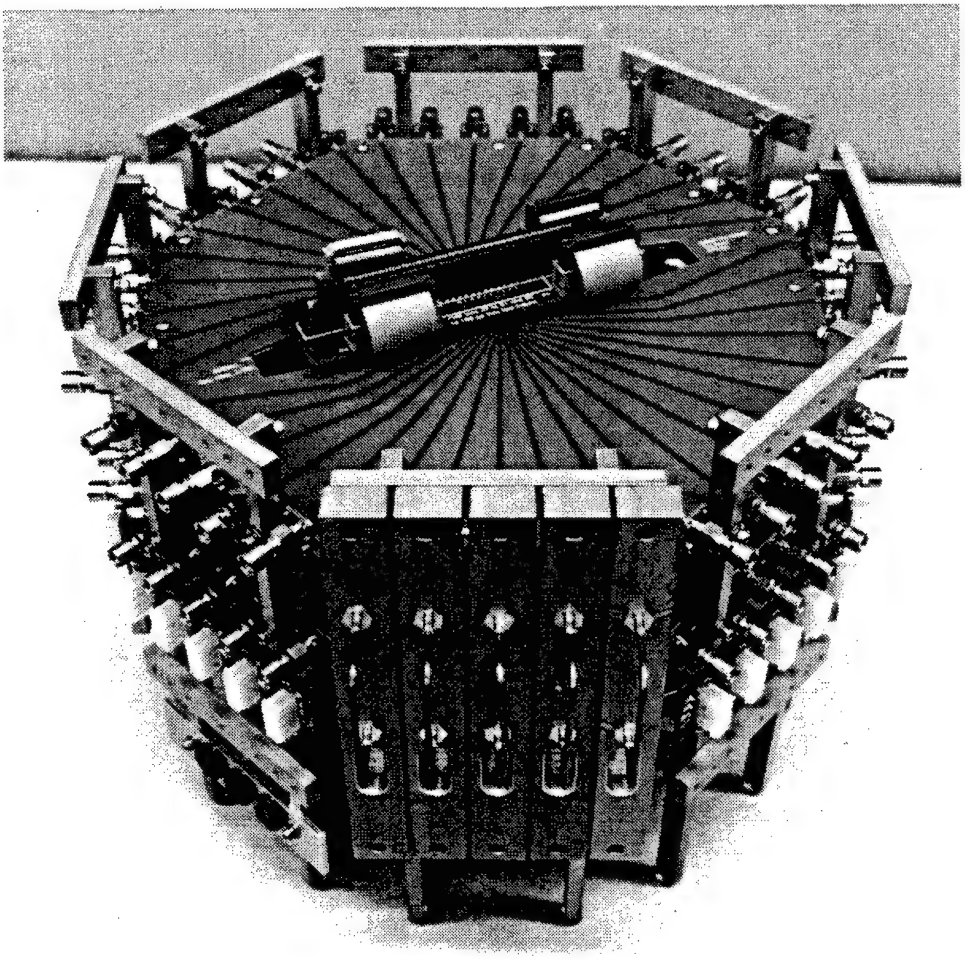


Figure 7.0-1: Picture of Through-Signal Adapters

interfering signals to power and ground lines, which introduced additional complications due to the very low impedance of the power and ground. At the low frequency end, we found a power operational amplifier with an operating frequency range between DC and 100 MHz that could supply 500 milli-amperes of current across that frequency range. This device was capable of providing the interfering signal used with low impedance power and ground currents. We also found a high speed operational amplifier with a specified upper frequency limit of 200 MHz. Above that frequency some type of microwave combiner was needed, and we developed a diplexer that would operate from about 500 KHz to almost 18 GHz with reasonable response. We also furnished a series of diplexer combiners that include wide-band amplifiers with frequency response from 500 MHz to 18 GHz, each having between one and two octaves of bandwidth. This was done in order to furnish higher RF power than most sweep or signal generators would be able to furnish without the use of an external amplifier.

7.1.1 Diplexer Signal Combiner Development

The design of the diplexer began by developing the RF performance specification. It was to be a three port device with a digital signal input, an interfering signal input, and an output that is a composite of the two inputs. If the signal path from the tester to the device under test happened to be bi-directional, the signal should also be able to travel both directions. There was to be low attenuation, on the order of 3 dB, between the interfering RF signal input and the output. There was to be low attenuation, at the digital frequency, between the digital signal input and the output. There was to be good isolation, on the order of 20 dB, of attenuation between the digital input and the interfering signal input.

A diplexer was designed to cover the high end of the frequency range. The diplexer utilizes micro-strip transmission line technology, microwave capacitors and inductors for isolation between the relatively low frequency range of the digital signal and the high frequency range of the interfering RF signal. In order to test various parts of the circuit, several prototype versions of the diplexer were designed and built. The printed circuit layout of the prototype RF circuit diplexer is shown in Figure 7.1.1-1. The frequency response of the circuit as a continuous 50 Ohm line is shown in Figure 7.1.1-2, and the response of the circuit including a 33 pf capacitor bridging a gap in the 50 ohm line is shown in Figure 7.1.1-3. The circuit was modeled and simulated, and the results of the simulation of the 50-ohm line are shown in Figure 7.1.1-4. The performance comparison between the model and the prototype was pretty good, which gave us confidence in the circuit. Some additional modeling was done to fine-tune parts of the design, and the final modeling schematic is shown in Figure 7.1.1-5. A schematic that is easier to relate to the diplexer physical layout of the diplexer is shown in Figure 7.1.1-6. The circuit layout needed to be physically changed in order to match the layout envelope allocated for the diplexer as well as all other combiners. The circuit was laid out shown in Figure 7.1.1-7, and a photograph of the finished diplexer is shown in Figure 7.1.1-8.

The S21 performance of a typical production diplexer is shown in Figure 7.1.1-9 and the S21 performance charts of all the production diplexers are shown in Appendix H. The performance of all the diplexers was measured from 500 MHz to 20 GHz, and this is shown on pages A1 to A5. Then, when it was determined that the devices would be used at frequencies below 500 MHz, diplexers 1-1, 2-2, and 2-7 were characterized from 300 KHz to 3 GHz as shown on page A6. As predicted by the simulation, there are several sharp dips in the performance of the completed diplexer between 3 and 4 GHz. Because they are so narrow, these dips should not cause a big problem, but there is between 4 and 8 dB of ripple in the performance of the devices between 6 GHz and the roll-off frequency, which is around 12 GHz for most of the units. The diplexers utilize right angle connectors and they are physically larger than the original prototype. They also include a surface-mount chip inductor rather than using two loops of gold wire to provide the inductance for the low-pass filter in the input signal to composite output path. These differences might account for some of the performance differences between the computer model, the prototype, and the actual diplexer circuit. The low frequency performance of several diplexers was measured, and it is shown in Figure 7.1.1-10 for a typical diplexer. As the figure shows, the useable performance of the diplexer extends down to about 300 MHz.

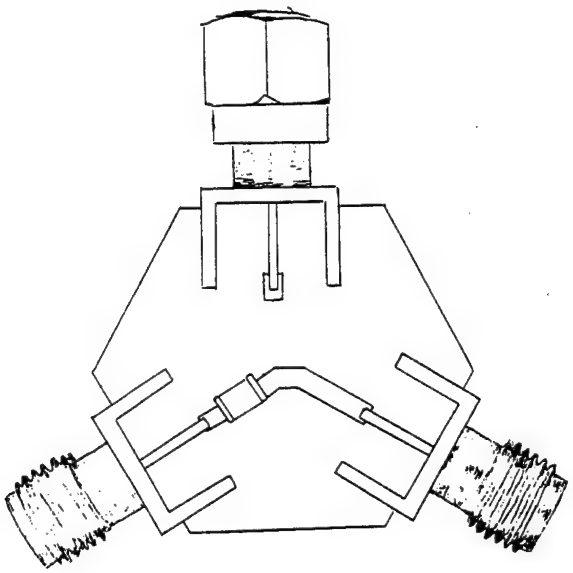


Figure 7.1.1-1: Prototype Diplexer Layout

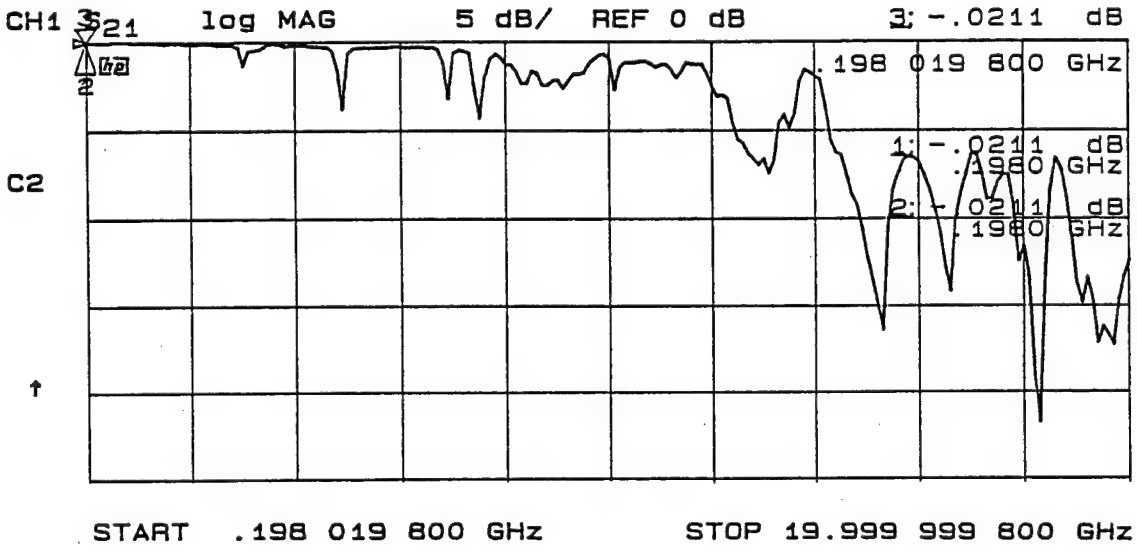


Figure 7.1.1-2: RF Response of Prototype Diplexer Circuit – Continuous 50 Ohm Line

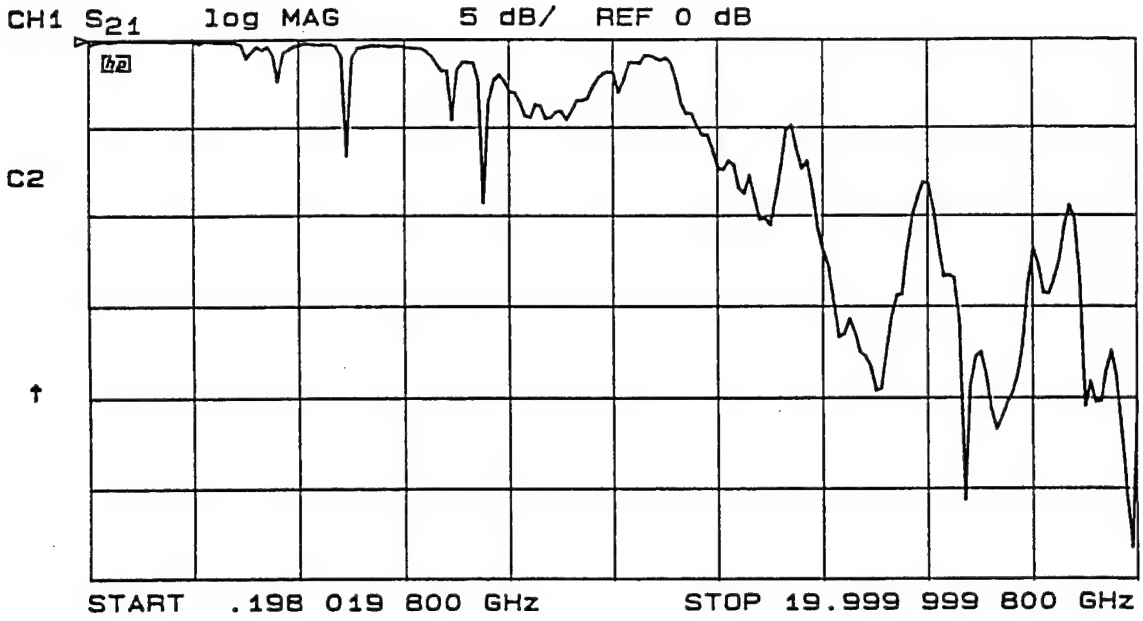


Figure 7.1.1-3: RF Response of Prototype Diplexer Circuit – 33 pf Cap. Bridging 50 Ohm Line

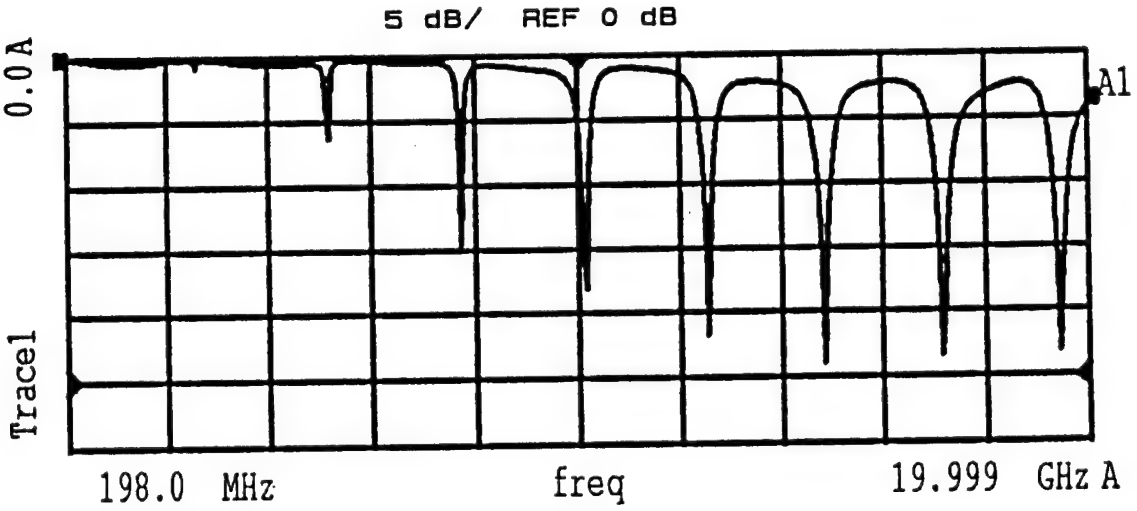


Figure 7.1.1-4: Prototype Diplexer – Results of Simulation of 50 Ohm Line

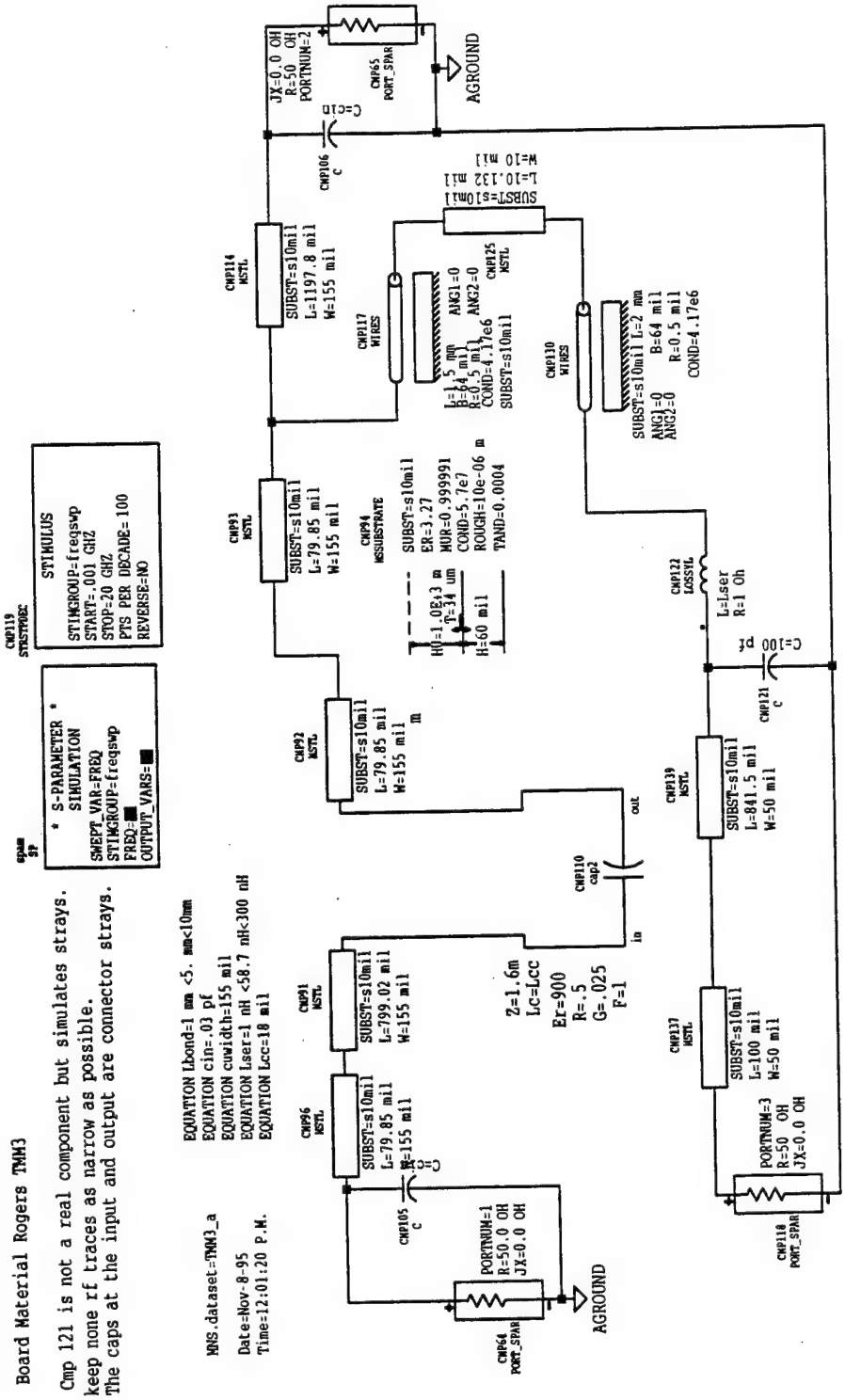


Figure 7.1.1-5: Modeling Schematic of Diplexer

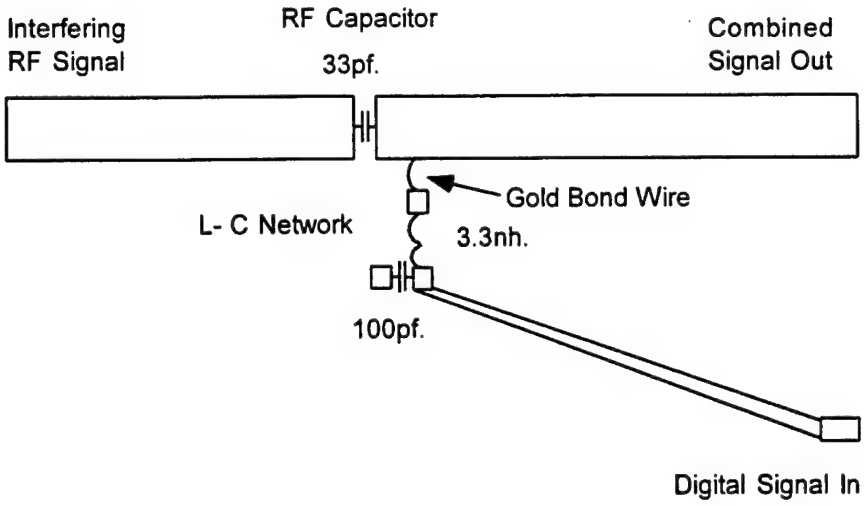


Figure 7.1.1-6: Layout/Schematic of Diplexer

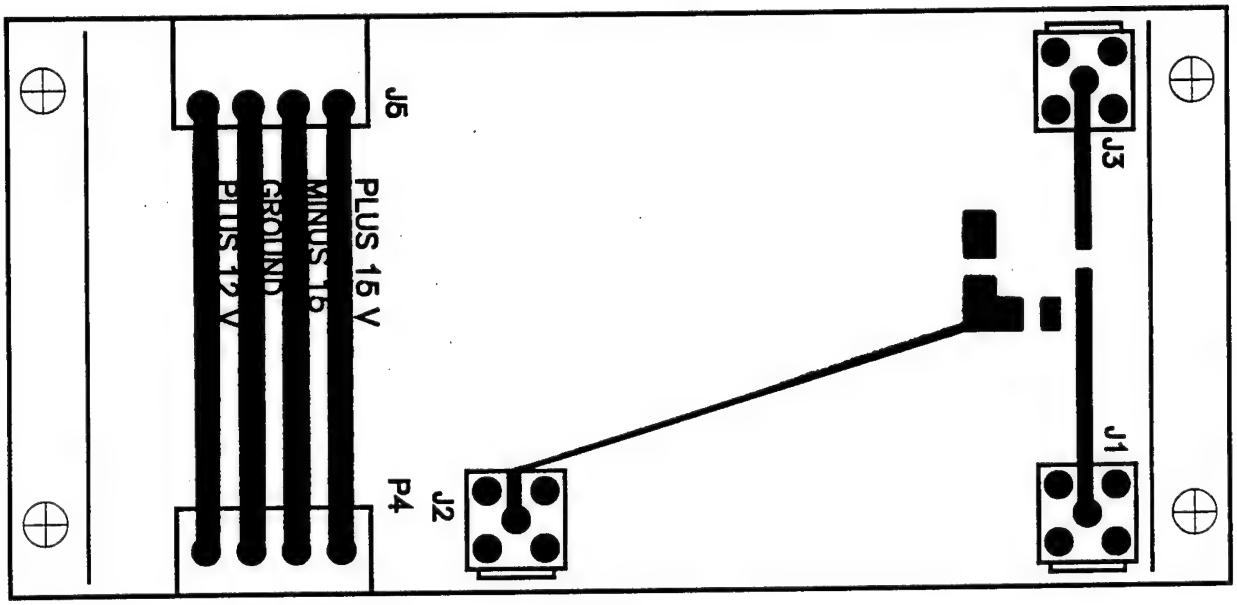


Figure 7.1.1-7: Layout of Diplexer Signal Combiner

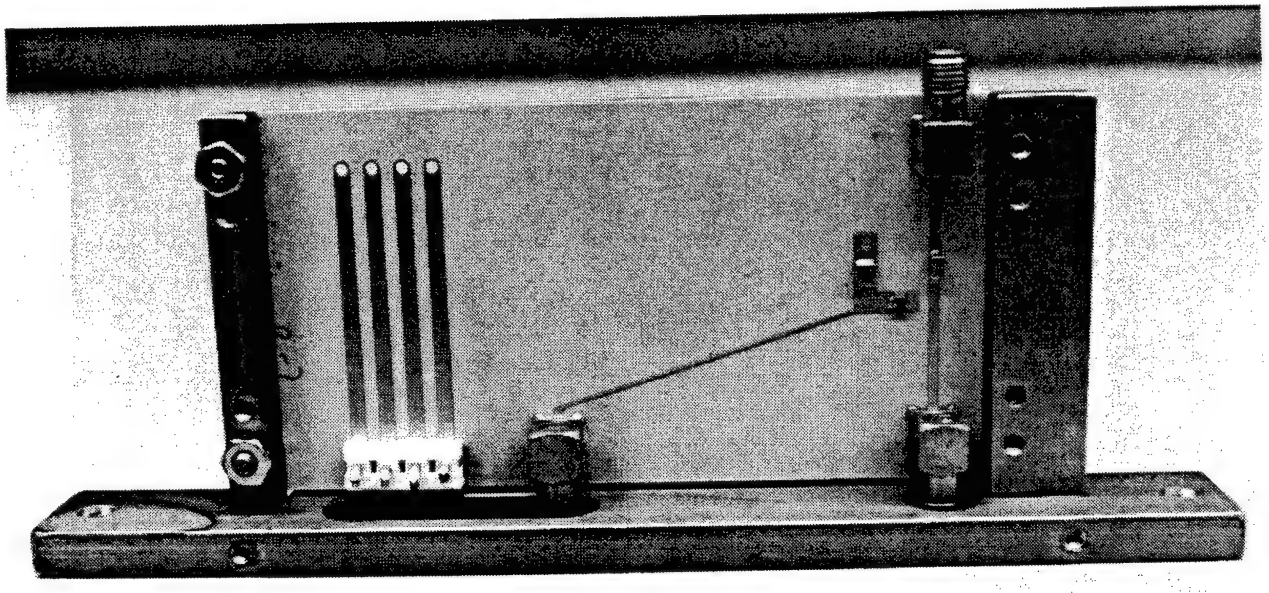


Figure 7.1.1-8: Photograph of Diplexer Signal Combiner

During its development, the diplexer was tested with 2 watts of RF power transmitted between the interfering RF input and the composite output. During conducted mode testing it was necessary to increase the interfering RF power to 20 watts at a number of frequencies in order to affect the operation of the devices under test. Because the design of the path between the interfering input and the composite output, which appears to be quite robust, consists of two sections of 50 ohm micro-strip transmission line and a coupling capacitor, and there was no problem handling that 20 watts of RF power. Six of the diplexers are used as diplexer signal combiners.

7.1.2 Diplexer/Wide-band Amplifier Signal Combiner Development

In order to increase the power of the interfering signal in the diplexer design without adding external TWT amplifiers we designed a combination diplexer/wide-band amplifier. We utilized some of the diplexers whose design was described in Section 7.1.1 and added wide-band amplification to the interfering signal. We designed these parts into a mechanical package that allowed the amplifier to fit within the mechanical envelope specified for the signal combiners. Since the wide-band amplifiers require DC power, this signal combiner required that a power plug and additional circuit traces be added to the basic diplexer design. The wide-band amplifier could only be used in the interfering signal leg because of the need to ensure signal integrity of the digital signal. We found wide-band amplifiers with 1 watt and 2 watts of output power that would fit within the signal combiner envelope. The mounting plate to which the amplifiers are attached provides additional cooling, but an external source of cooling air during extended test periods might be advisable. A layout of the diplexer/wide-band

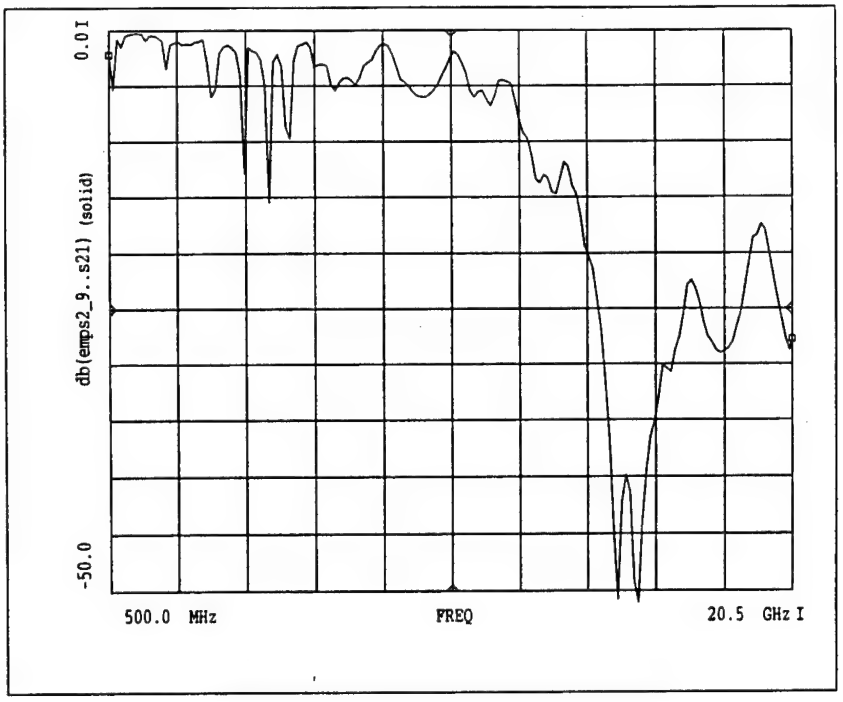


Figure 7.1.1-9: S21 Performance of Typical Diplexer

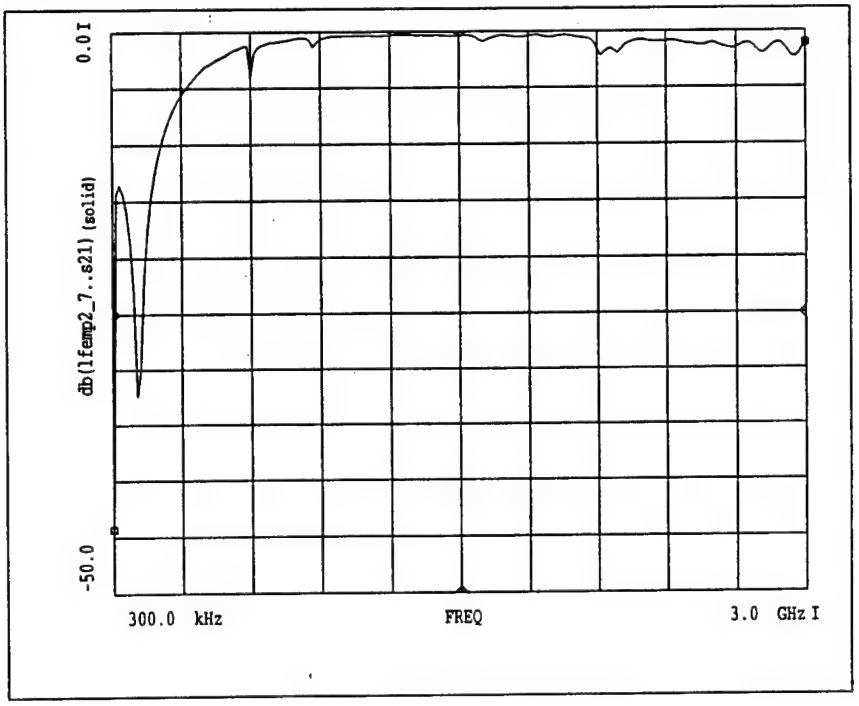


Figure 7.1.1-10: Low Frequency Performance of Typical Diplexer

amplifier is shown in Figure 7.1.2-1 and a photograph is shown in Figure 7.1.2-2. The selection of wide-band amplifiers, with their major size and performance specifications, is shown in Figure 7.1.2-3. The gain from interfering signal input through the wide-band amplifier to combined output at a number of frequencies across the useable frequency band is shown in Figure 7.1.2-4. The complete data sheets for all of the wide-band amplifiers is shown in Appendix J.

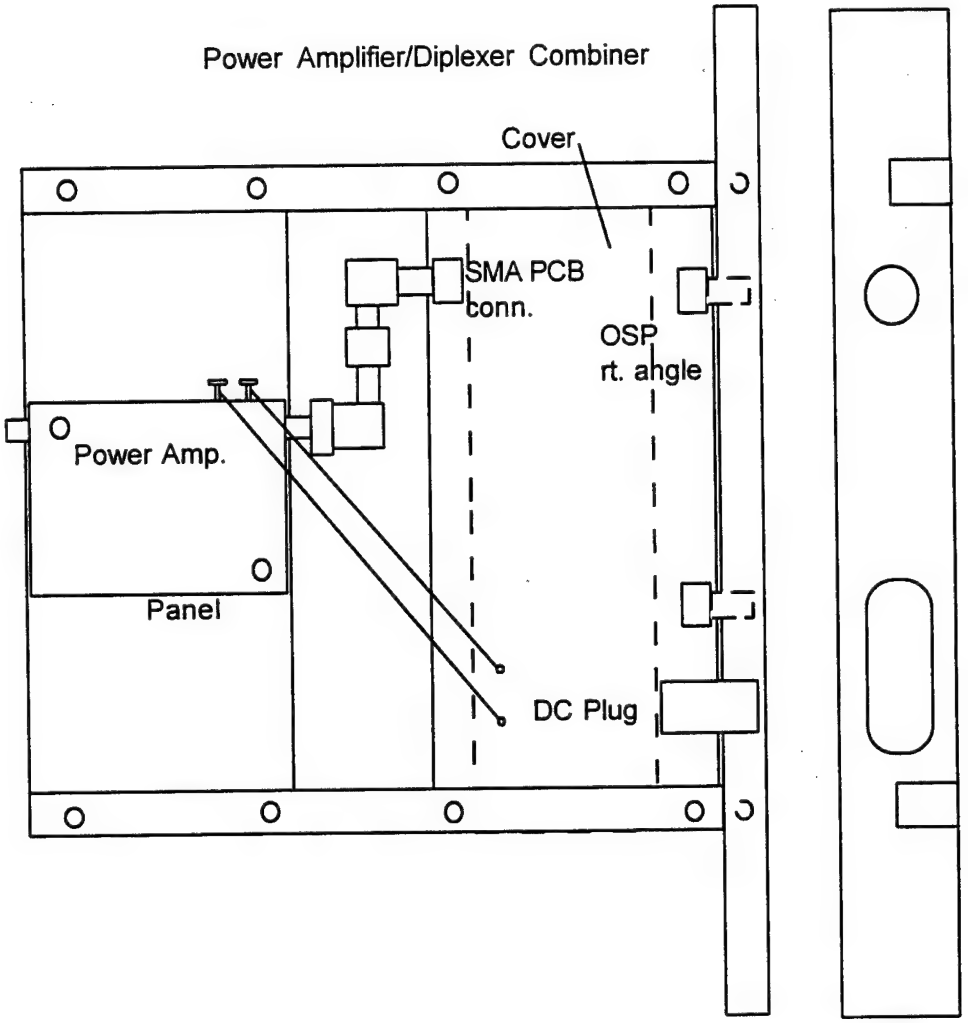


Figure 7.1.2-1: Layout of Diplexer/Wide-band Amplifier

7.1.3 High Speed Op Amp Signal Combiner Development

It is desirable to have an operational amplifier combiner so that interfering signals between DC and about 150 MHz could be generated. Diplexer signal combiners are not that good in the low frequency region because of their capacitive coupling. Operational amplifiers that could be used in this

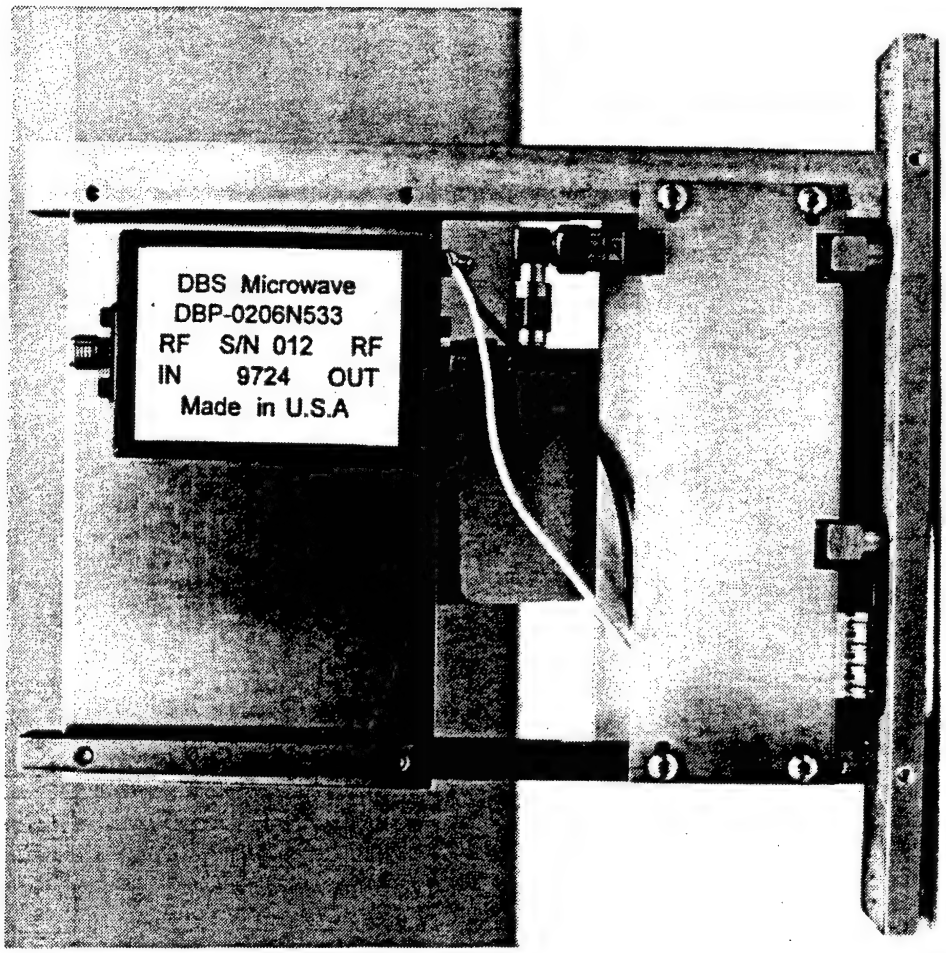


Figure 7.1.2-2: Photograph of Diplexer/Wide-Band Amplifier

Frequency					Output				+15V Current
Range, GHz		Mfg.	Model	Gain	RF pwr.	Case Size, Inches			Required
0.5	2	DBS	DBP-0102N533	40dB	2 W	0.67	1.56	2.91	1.4 Amp
2	6	DBS	DBP-0206N533	30dB	2 W	0.67	1.56	2.91	2 Amp
2	8	Cernex	CPA02083030	30dB	1 W	0.38	0.93	3.25	1.1 Amp
6	18	DBS	DPT-18616	32dB	1 W	0.67	1.56	3.66	2.5 Amp

Figure 7.1.2-3: Wide-Band Amplifier Specifications

W/B Amp P/N	S/N	Diplexer	Frequency	Gain
DBP18616	1	1-2	6	35
			9	32.5
			12	30.4
			15	15.5
			16	12.3
DBP18616	2	1-3	6	33.5
			9	29.5
			12	30
			15	20
			17	4
DBP0206N533	12	2-1	2	34.4
			4	30.6
			6	26.8
DBP0206N533	13	3-1	2	35.7
			4	32.8
			6	32.8
CPA02063230	2346	2-9	2	42.7
			4	42.8
			6	40.7
CPA02063230	2347	1-5	2	41.4
			4	38.5
			6	38.9
CPA02063230	2348	2-8	2	39.1
			4	37.9
			6	38.7
DBP0102N533	7	2-5	0.5	41.6
			1	43.7
			1.5	40.5
			2	40.3
DBP0102N533	8	2-6	0.5	41.8
			1	44.8
			1.5	42.1
			2	42.6
DBP0102N533	9	1-6	0.5	39.6
			1	40.9
			1.5	34.5
			2	35.9
DBP0102N533	10	2-4	0.5	40.9
			1	40
			1.5	35.5
			2	35.4

Figure 7.1.2-4: Gain Through Combined Diplexer/Wide-Band Amplifier

application need to be unity gain stable, have a low impedance (high current) output, have a voltage output swing of at least 10 volts, and be as fast as possible. During the preliminary design stage we found many high-speed amplifiers, but most did not have a wide enough output voltage, and most would not drive a 50 ohm load. An output voltage range of at least 10 volts is needed because the combiner has to replicate a digital signal of approximately 0 to 5 volts and have a substantial reserve in each direction to accommodate a large interfering signal. We finally settled on the Comlinear/National CLC232 operational amplifier. It has an output voltage range of +/- 11 volts with +/- 15 volt power supplies, and at 10 volts out, the bandwidth is almost 200 MHz at room temperature. The circuit diagram is shown in Figure 7.1.3-1. A photograph of a high-speed operational amplifier signal combiner is shown in Figure 7.1.3-2 and the top side layout of the printed circuit board is shown in Figure 7.1.3-3. The CLC-232 does require a heat sink for proper thermal operation, and we did find a heat sink that fits within the mounting envelope. During acceptance testing we found that the production board has a bandwidth of almost 170 MHz at a digital output of 5 volts peak to peak and over 0.5 volt of RF, and it appears to satisfy all of our requirements. The voltage output due to the RF interfering signal does vary somewhat with frequency.

The high speed Op-Amp combiners are furnished in two different configurations: Four of the combiners are furnished with 50 ohm terminating resistors at the RF interfering signal input. RF signals up to approximately 3 Volts RMS may be used with these devices because of the limited power dissipation of the 50-ohm on-board termination. The rest of the combiners have the RF interfering signal input terminated at 200 ohms in order to accommodate higher voltage interfering signals.

7.1.4 High Power Op Amp Signal Combiner Development

A high power operational amplifier signal combiner was needed to inject an interfering signal into DC power and ground lines. An operational amplifier that is suitable for this application needs to be unity gain stable, have a very low impedance output, have a voltage output swing of at least 10 volts, and still be as fast as possible. We found a high power, high speed operational amplifier and a high power high speed buffer, both manufactured by Apex. We chose the operational amplifier instead of the buffer because of a simpler overall design and, except for slew rate, comparable performance.

The high power operational amplifier signal combiner needs to meet about the same requirements as the high-speed operational amplifier combiner, with the addition of being able to supply more output current in order to drive a lower output impedance load. The final circuit design of the high power op-amp combiner is shown in Figure 7.1.4-1. The topside layout of the printed circuit board is shown in Figure 7.1.4-2. Because of it's high output power, the high power operational amplifier consumes a lot of DC power from the power supplies. Therefore, a good heat-sink design was necessity to dissipate the heat. The design uses standard heat sink "bar stock" to minimize the number of machine cuts. We were able to lay out the circuit board and fit both the circuit board and heat sink within the specified mechanical envelope. The production high power signal combiner has a bandwidth of about 90 MHz at about 500 ma. power output.

The high power operational amplifier combiners are furnished in two different configurations: Four of the combiners are furnished with 50 ohm terminating resistors at the RF interfering signal

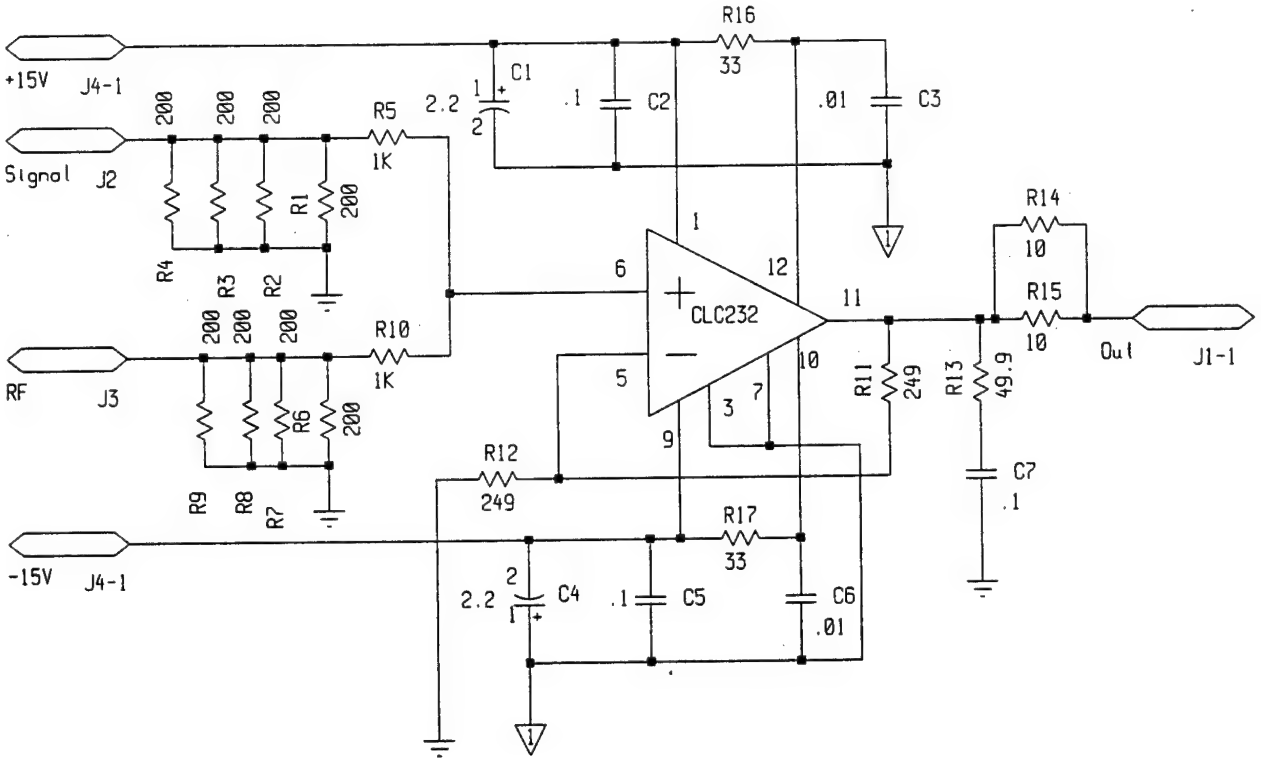


Figure 7.1.3-1: Circuit Diagram of High Speed Operational Amplifier Combiner

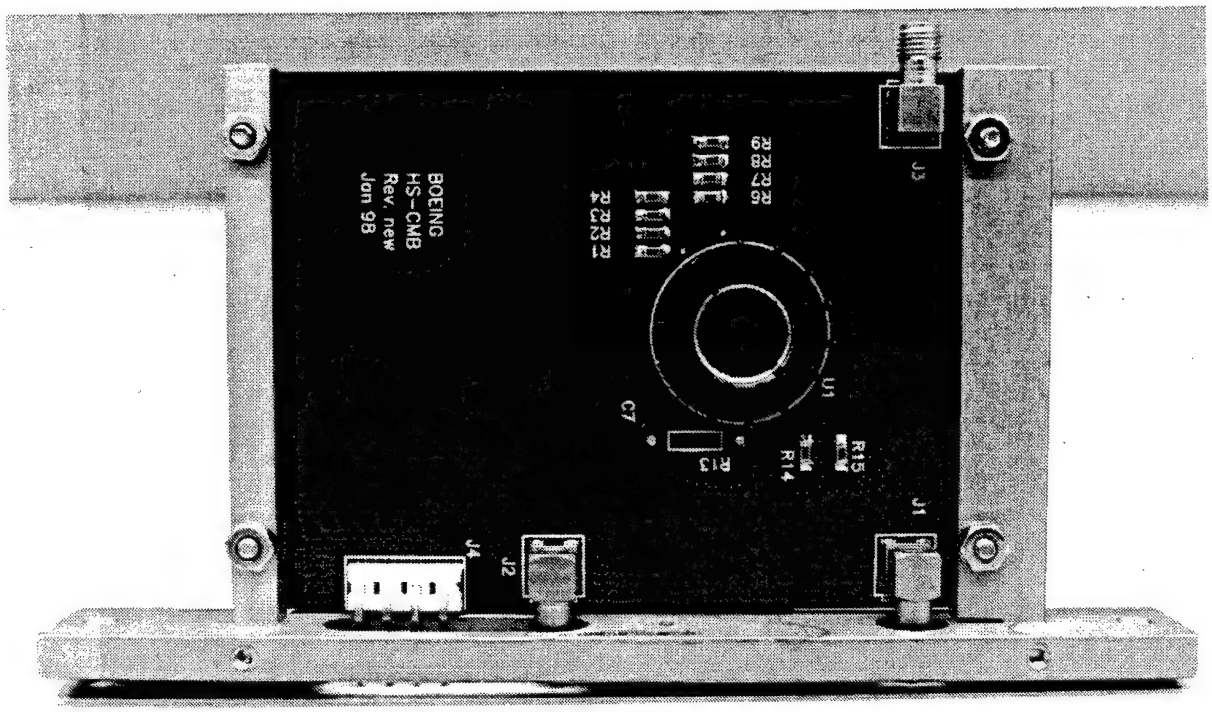


Figure 7.1.3-2: Photograph of High Speed Operational Amplifier Combiner

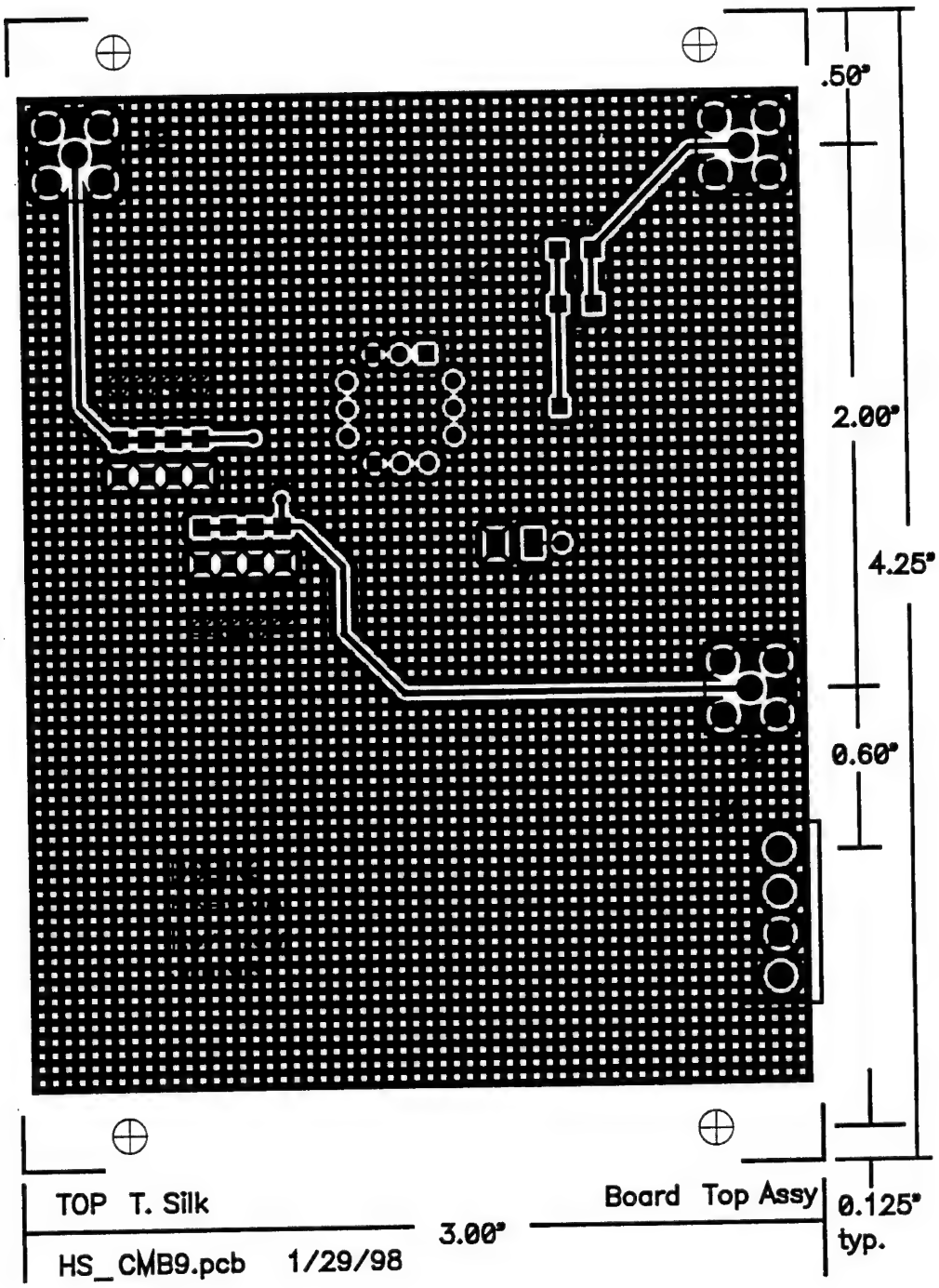


Figure 7.1.3-3: Top Side Printed Circuit of High Speed Operational Amplifier Combiner

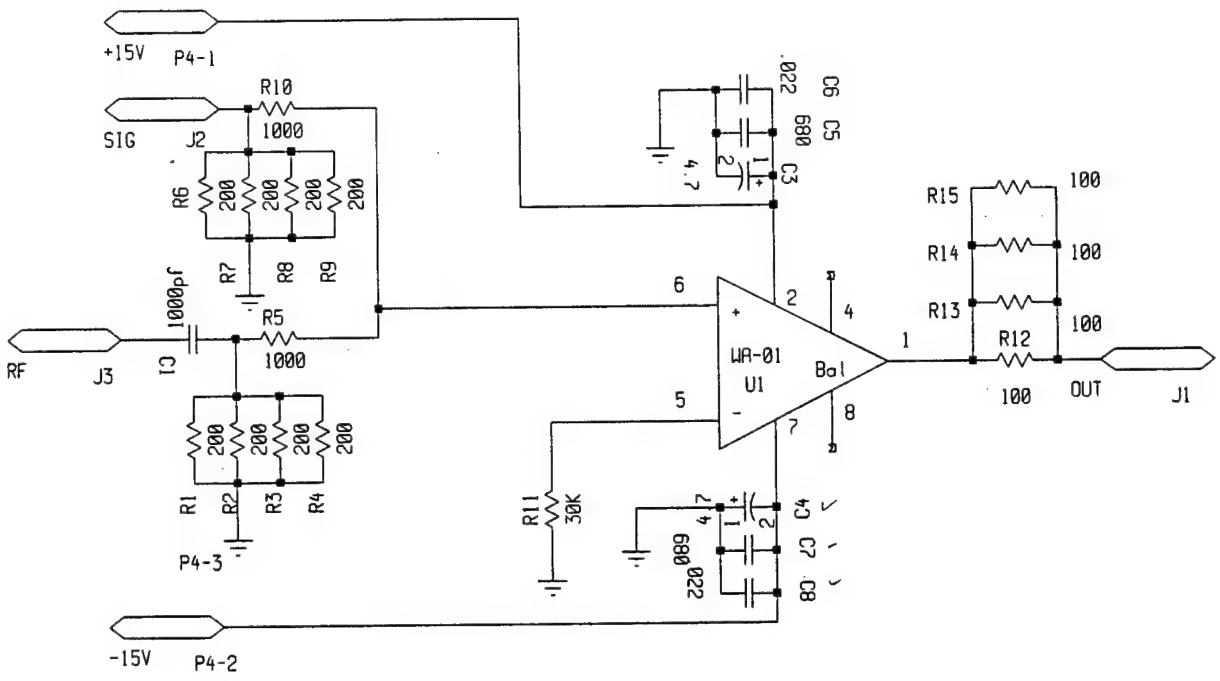


Figure 7.1.4-1: Schematic of High Power Operational Amplifier Combiner

input. RF signals up to approximately 3 Volts RMS may be used with these devices because of the limited power dissipation of the 50-ohm on-board termination. The rest of the boards, have the RF interfering signal input terminated at 200 ohms in order to accommodate higher voltage interfering signals. A photograph of a high power operational amplifier signal combiner is shown in Figure 7.1.4-3.

7.1.5 Power Measurement Test Fixture Development

During the design of the test fixture, we knew there was going to be an impedance mis-match when looking into the device under test, because of the high characteristic input impedance of CMOS digital gates. As a tool to help us determine how serious the impedance mis-matches are and whether they are affecting the validity of our measurements, we designed an adapter that includes a bi-directional power divider. With the measurement fixture inserted between the test fixture and one of our standard signal combiners, it should be possible to determine the amount of RF power being transmitted into the circuit under investigation, and how much is being reflected back. In addition to this fixture, several RF power meters will be required to determine the forward and reflected power levels. Because we are not matching to 50 ohms at the output of the test fixture, the measured power readings might not be accurate, and it might take some calculating to determine the exact amount of power.

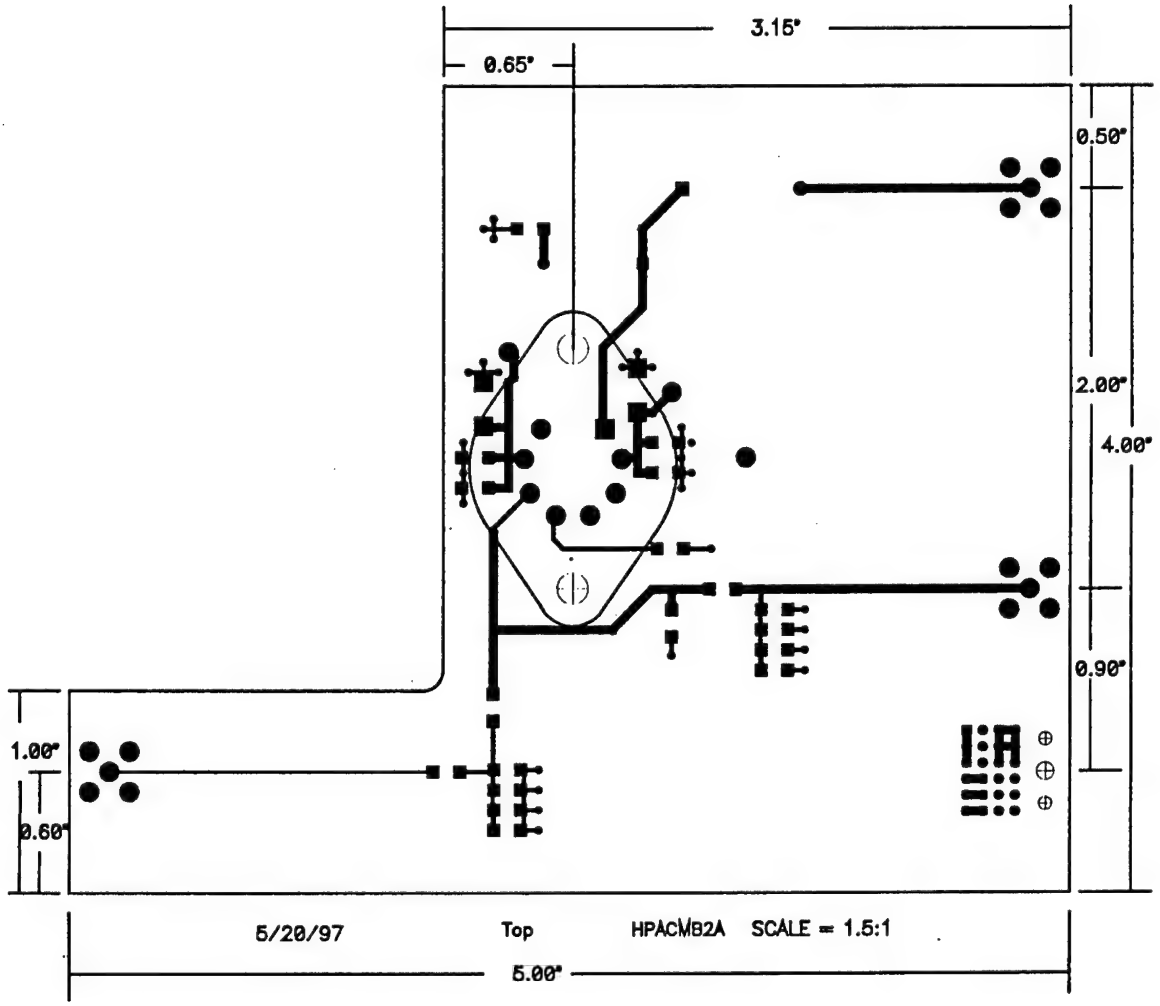


Figure 7.1.4-2: Top Side Layout of High Power Operational Amplifier Combiner

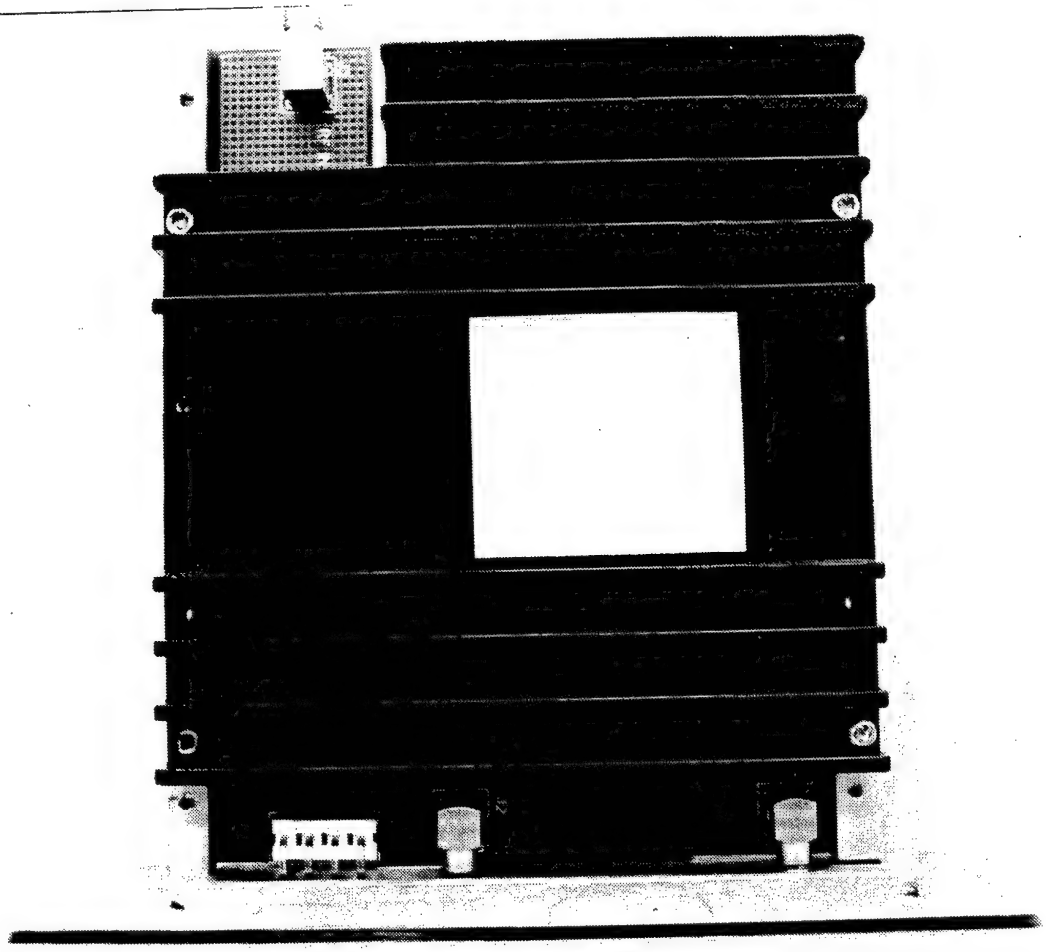


Figure 7.1.4-3: Photograph of High Power Operational Amplifier Signal Combiner

8.0 CONCLUSIONS

This research effort was undertaken to assess the susceptibility of advanced packaged devices to the effects of electromagnetic radiation. It was also hoped that we would be able to learn a number of design techniques that might mitigate the effects of electromagnetic radiation. Based on the results of this research, the following conclusions are presented:

1) There is reasonable correlation between simulated and observed upset levels for the simulation and testing that was completed as part of this contract. This correlation was quite good in some cases but not so good in others. Where the correlation is not so good we would suspect that more attention needs to be paid in developing accurate models of the part in question.

2) The test fixture and signal combiners provided under this contract are adequate to test the 3DMM and memory-only PMM for electromagnetic susceptibility. Through the use of additional test fixtures, (one additional set type is included with the test fixture), other types of electronic devices, especially digital devices, may be tested for susceptibility to conducted electromagnetic energy.

3) The ability of current software tools to convert design data of complex electronic devices into electrical models is lacking. We found that the ability of the software tools we used, which use the Finite Element Method, to calculate the circuit characteristics of high aspect ratio circuits, such as those with long thin circuit board traces, is very limited at this time. The software could handle very small or simple structures, but structures of the type we tried to analyze created mesh structures so large that they failed to converge on a solution after more than 50 hours of workstation CPU time. However, once a model has been created, the software tools to analyze the circuit and calculate the response to input signals seem to be quite good.

4) Testing performed on the 3DMM indicates that if interference gets onto the DC power lines, it can easily spread and affect nearly every circuit within a packaged device.

5) If an interfering signal that is being applied to a particular circuit is close to it's susceptibility threshold, an interfering signal applied to another part of the circuit would not have to be very large in order cause failure in the operation of the circuit.

6) Although only digital devices were tested, the susceptibility of analog devices could also be measured through the use of the EMEAP test fixture and a suitable automated analog circuit tester.

7) Modeling and simulation results of the 3DMM show that a 0.8 to 1.0 volt signal at 100 MHz will cause the circuit to upset. Even at 10 GHz the noise voltage must be increased by only 4 dB to cause upset. down. But at 18 GHz the level of noise would have to be greater than 4000 Volts to propagate a 0.8 volt signal to the die.

8) The test results of the 3DMM do not exactly conform to the simulated results. The susceptibility at 100 MHz is quite low, but it increases more rapidly than shown by the modeling results.

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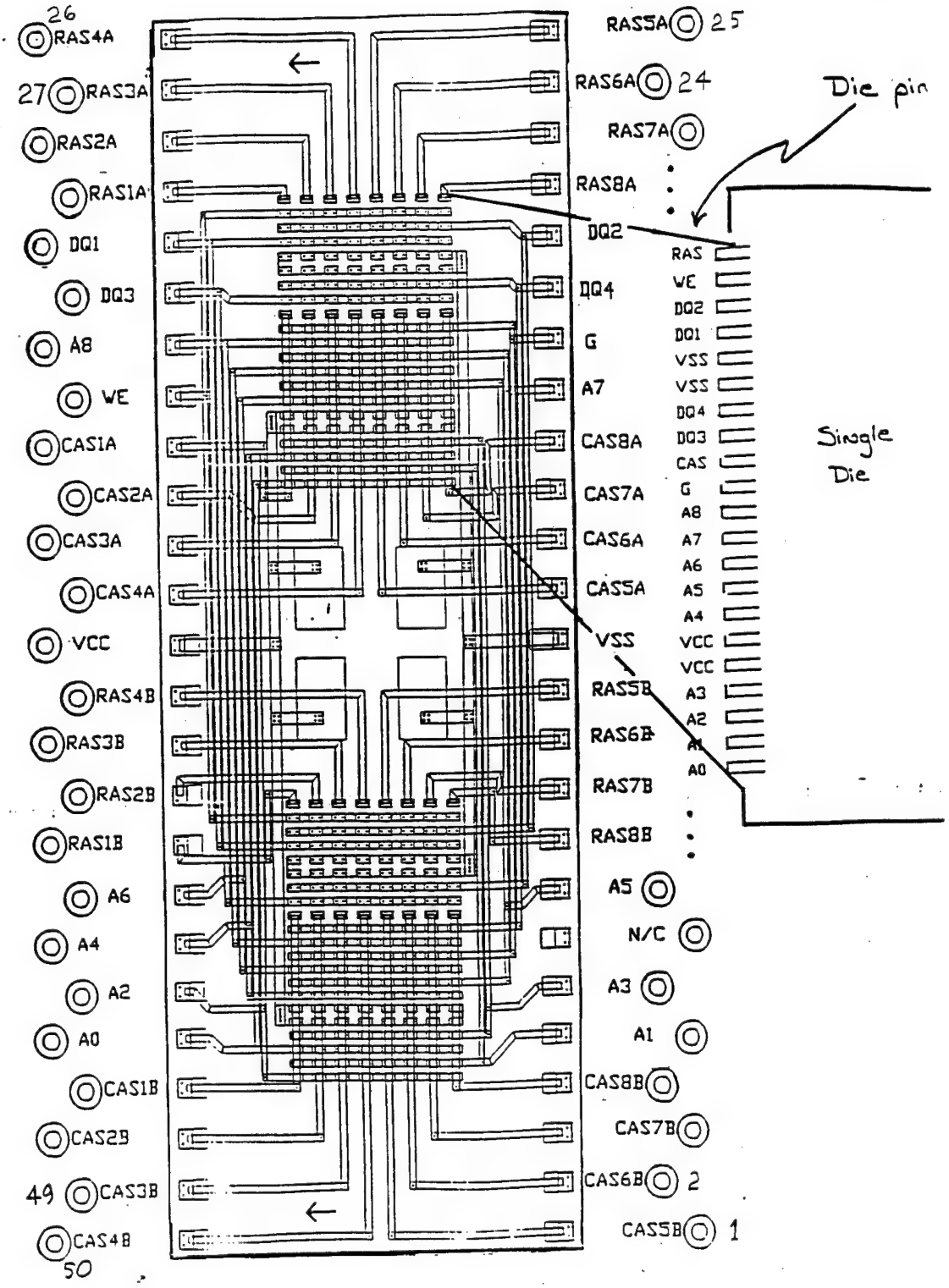
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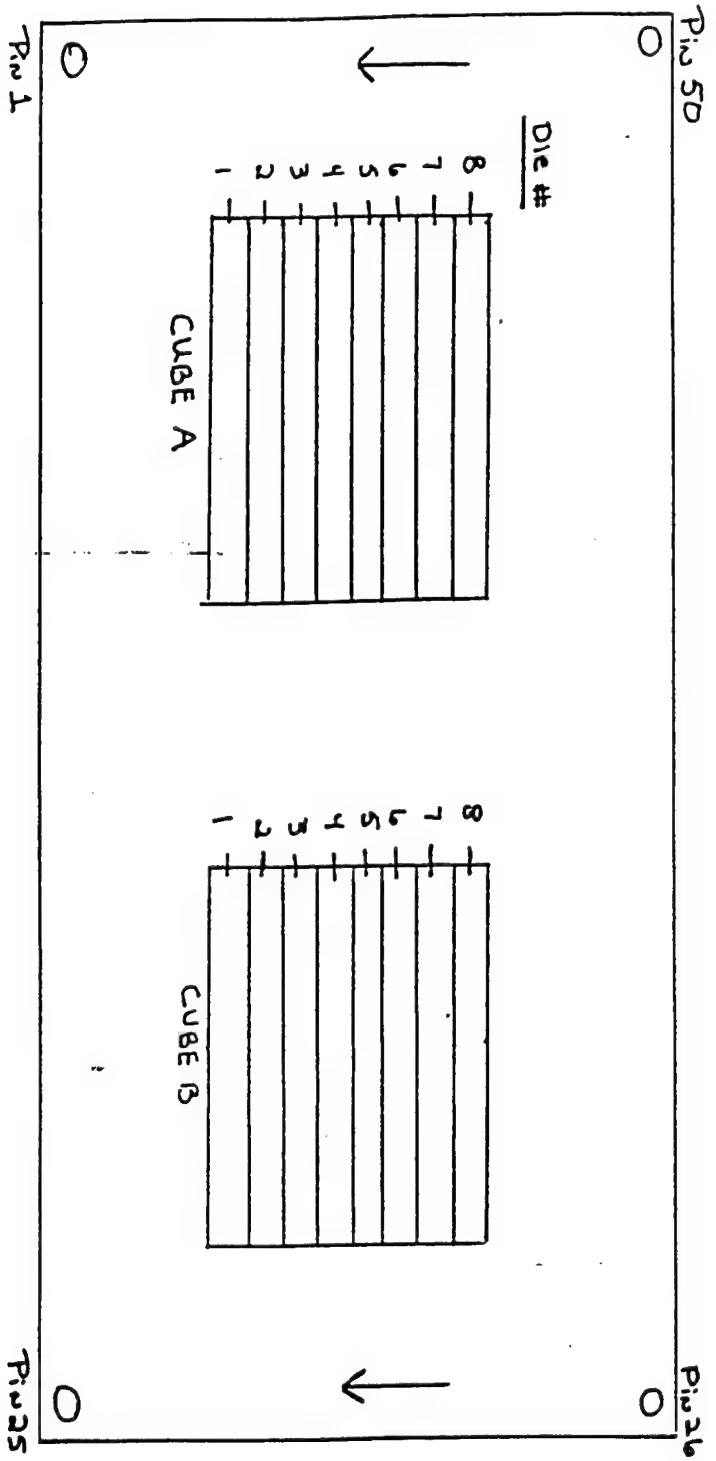
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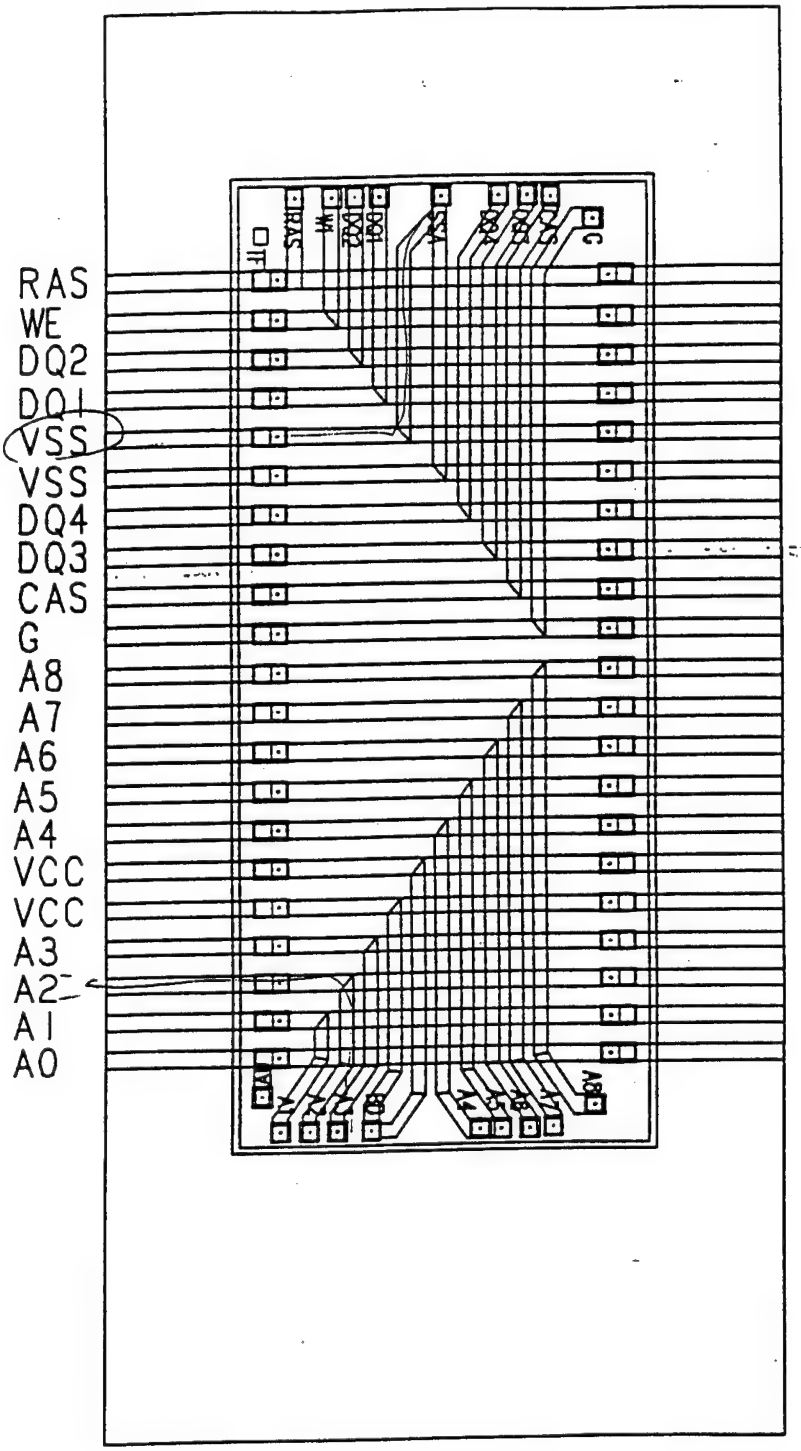
CUBE B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A0
DRAM ROUTING

TMS44C256
262 144-WORD BY 4-BIT
DYNAMIC RANDOM-ACCESS MEMORY

SMGS256C — JUNE 1986 — REVISED NOVEMBER 1990

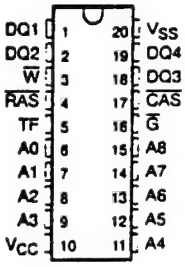
This data sheet is applicable to all TMS44C256s symbolized with Revision "D" and subsequent revisions as described on page 5-21.

- **262 144 × 4 Organization**
- **Single 5-V Supply (10% Tolerance)**
- **Performance Ranges:**

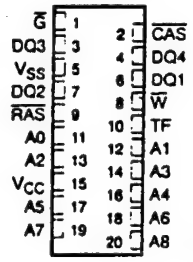
	ACCESS TIME $t_{a(R)}$ (t_{RAC}) (MAX)	ACCESS TIME $t_{a(C)}$ (t_{CAC}) (MAX)	ACCESS TIME $t_{a(CA)}$ (t_{CAA}) (MAX)	READ OR WRITE CYCLE (MIN)
TMS44C256-60	60 ns	15 ns	30 ns	110 ns
TMS44C256-70	70 ns	18 ns	35 ns	130 ns
TMS44C256-80	80 ns	20 ns	40 ns	150 ns
TMS44C256-10	100 ns	25 ns	45 ns	180 ns
TMS44C256-12	120 ns	30 ns	55 ns	220 ns

- **Enhanced Page Mode Operation with $\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . . 512-Cycle Refresh In 8 ms (Max)**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **Texas Instruments EPIC™ CMOS Process**
- **All Inputs and Clocks Are TTL Compatible**
- **High-Reliability Plastic 20-Pin 300-Mil-Wide DIP, 20/26 J-Lead Surface Mount (SOJ) ('44C256-60 and '44C256-70 Available in SOJ Only), 20/26 J-Lead Thin Surface Mount (ThinSOJ), or 20-Pin Zig-Zag In-Line (ZIP) Packages**
- **Operation of TI's Megabit CMOS DRAMs Can Be Controlled by TI's SN74ALS6301 and SN74ALS6302 Dynamic RAM Controllers**
- **Operating Free-Air Temperature . . . 0°C to 70°C**

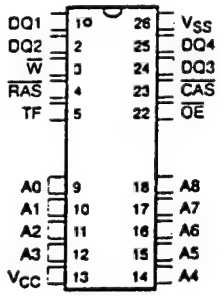
N Package
(Top View)



SD Package
(Top View)



DJ and DN Packages†
(Top View)



†The packages shown here are for pinout reference only. The DJ package is actually 75% of the length of the N package.

PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ4	Data In/Data Out
$\overline{G}$	Data-Output Enable
$\overline{RAS}$	Row-Address Strobe
TF	Test Function
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

description

The TMS44C256 series are high-speed, 1 048 576-bit dynamic random access memories, organized as 262 144 words of four bits each. They employ state-of-the-art EPIC™ (Enhanced Process Implanted CMOS) technology for high performance, reliability, and low power at low cost.

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description (continued)

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, 80 ns, 100 ns, and 120 ns. Maximum power dissipation is as low as 305 mW operating and 11 mW standby on 120 ns devices.

The EPIC technology permits operation from a single 5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{CC} peaks are 140 mA typical, and a – 1-V input voltage undershoot can be tolerated, minimizing system noise considerations.

All inputs and outputs, including clocks, are compatible with Series 54/74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS44C256 is offered in a 20-pin dual-in-line (N suffix) package, a 20-pin zig-zag in-line (SD suffix) package, a 20/26 J-lead plastic surface mount SOJ (DJ suffix), and a 20/26 J-lead thin plastic surface mount SOJ (DN suffix). The TMS44C256-60 and TMS44C256-70 are available in the 20/26 J-lead plastic surface mount SOJ (DJ suffix) only. These packages are guaranteed for operation from 0°C to 70°C.

operation

enhanced page mode

Page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used. With minimum $\overline{CAS}$ page cycle time, all 512 columns specified by column addresses A0 through A8 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the TMS44C256 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as "enhanced page mode." Valid column address may be presented immediately after $t_{h(RA)}$ (row address hold time) has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after $t_{a(C)}$ max (access time from $\overline{CAS}$ low), if $t_{a(CA)}$ max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of $t_{a(C)}$ or $t_{a(CP)}$ (access time from rising edge of $\overline{CAS}$).

address (A0 through A8)

Eighteen address bits are required to decode 1 of 262 144 storage cell locations. Nine row-address bits are set up on pins A0 through A8 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then nine column-address bits are set up on pins A0 through A8 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the output buffer, as well as latching the address bits into the column-address buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from the standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle, permitting a write operation with $\overline{G}$ grounded.

data in (DQ1-DQ4)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{G}$ must be high to bring the output buffers to high-impedance prior to impressing data on the I/O lines.

data out (DQ1-DQ4)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ and $\overline{G}$ are brought low. In a read cycle the output becomes valid after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ and $t_{a(CA)}$ are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{G}$ are low. $\overline{CAS}$ or $\overline{G}$ going high returns it to a high-impedance state. This is accomplished by bringing $\overline{G}$ high prior to applying data, thus satisfying $t_{d(GHD)}$.

output enable ($\overline{G}$)

$\overline{G}$ controls the impedance of the output buffers. When $\overline{G}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{G}$ low during a normal cycle will activate the output buffers putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state. Once in the low-impedance state, they will remain in the low-impedance state until either $\overline{G}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every eight milliseconds to retain data. This can be achieved by strobing each of the 512 rows (A0-A8). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ [see parameter $t_{d(CLRL)R}$] and holding it low after $\overline{RAS}$ falls [see parameter $t_{d(RLCH)R}$]. For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally. The external address is also ignored during the hidden refresh option.

power-up

To achieve proper device operation, an initial pause of 200 µs followed by a minimum of eight initialization cycles is required after power-up to the full V_{CC} level.

test function pin

During normal device operation the TF pin must either be disconnected or biased at a voltage less than or equal to V_{CC}.

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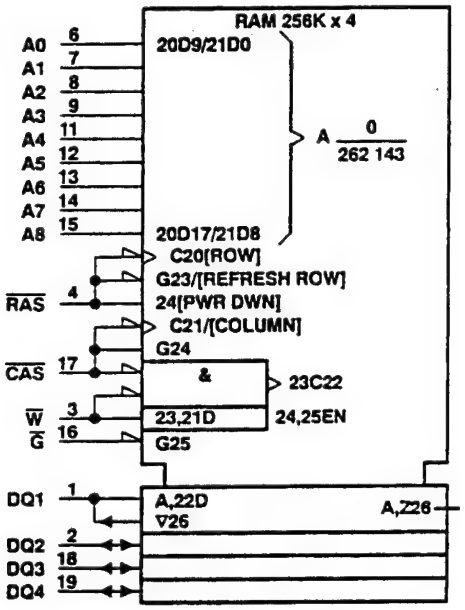
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the N package.

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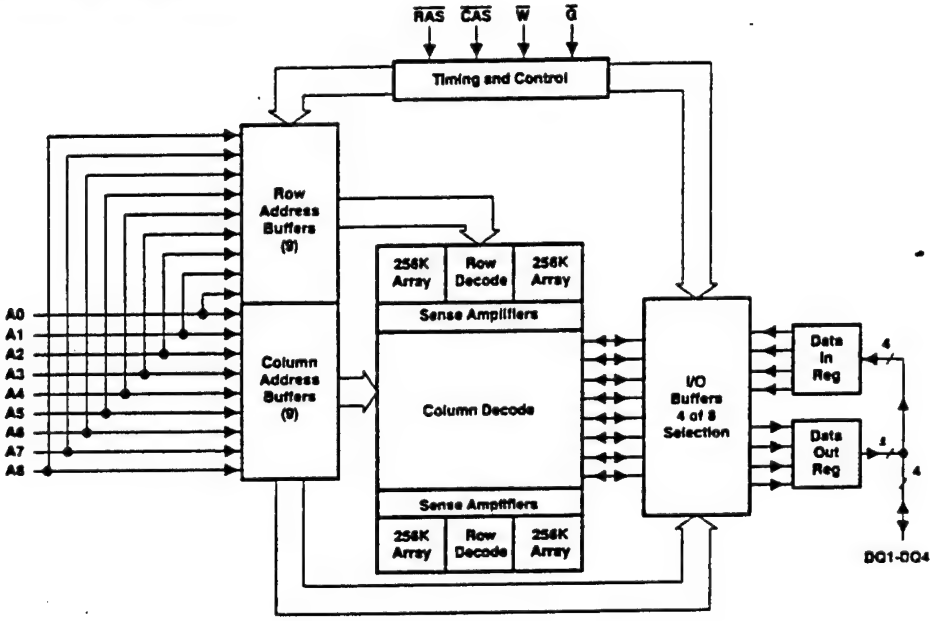
functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	6.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

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electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS44C256-60		TMS44C256-70		UNIT
			MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 5.8 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}		± 10		± 10	µA
I_O	Output current (leakage)	V_O = 0 V to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		± 10		± 10	µA
I_{CC1}	Read/write cycle current	$t_{c(rdW)}$ = minimum, V_{CC} = 5.5 V		95		80	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V		2		2	mA
I_{CC3}	Average refresh circuit ($\overline{RAS}$-only, or CBR)	$t_{c(rdW)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low, after $\overline{CAS}$ low (CBR)		90		80	mA
I_{CC4}	Average page current	$t_{c(P)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		70		60	mA

PARAMETER		TEST CONDITIONS	TMS44C256-80		TMS44C256-10		TMS44C256-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 5.8 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}	Read/write cycle current	$t_{c(rdW)}$ = minimum, V_{CC} = 5.5 V		75		65		55	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V		2		2		2	mA
I_{CC3}	Average refresh circuit ($\overline{RAS}$-only, or CBR)	$t_{c(rdW)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low, after $\overline{CAS}$ low (CBR)		70		60		50	mA
I_{CC4}	Average page current	$t_{c(P)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		50		45		35	mA

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			5	pF
$C_{i(W)}$	Input capacitance, write-enable input			5	pF
$C_{i(G)}$	Input capacitance, output-enable input			5	pF
C_O	Output capacitance			7	pF

NOTE 3: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)

PARAMETER		ALT. SYMBOL	TMS44C256-60		TMS44C256-70		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$ low	t_{CAC}		15		18	ns
$t_{a(CA)}$	Access time from column-address	t_{CAA}		30		35	ns
$t_{a(R)}$	Access time from $\overline{RAS}$ low	t_{RAC}		60		70	ns
$t_{a(G)}$	Access time from $\overline{G}$ low	t_{GAC}		15		18	ns
$t_{a(CP)}$	Access time from column precharge	t_{CAP}		35		40	ns
$t_{d(CLZ)}$	$\overline{CAS}$ low to output in low Z	t_{CLZ}	0		0		ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high (see Note 4)	t_{OFF}	0	15	0	18	ns
$t_{dis(G)}$	Output disable time after $\overline{G}$ high (see Note 4)	t_{GOFF}	0	15	0	18	ns

PARAMETER		ALT. SYMBOL	TMS44C256-80		TMS44C256-10		TMS44C256-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$ low	t_{CAC}		20		25		30	ns
$t_{a(CA)}$	Access time from column-address	t_{CAA}		40		45		55	ns
$t_{a(R)}$	Access time from $\overline{RAS}$ low	t_{RAC}		80		100		120	ns
$t_{a(G)}$	Access time from $\overline{G}$ low	t_{GAC}		20		25		30	ns
$t_{a(CP)}$	Access time from column precharge	t_{CAP}		40		50		60	ns
$t_{d(CLZ)}$	$\overline{CAS}$ low to output in low Z	t_{CLZ}	0		0		0		ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high (see Note 4)	t_{OFF}	0	20	0	25	0	30	ns
$t_{dis(G)}$	Output disable time after $\overline{G}$ high (see Note 4)	t_{GOFF}	0	20	0	25	0	30	ns

NOTE 4: $t_{dis(CH)}$ and $t_{dis(G)}$ are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

PARAMETER		ALT. SYMBOL	TMS44C256-60		TMS44C256-70		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time (see Note 6)	t_{RC}	110		130		ns
$t_{c(W)}$	Write cycle time	t_{WC}	110		130		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	155		181		ns
$t_{c(P)}$	Page-mode read or write cycle time (see Note 7)	t_{PC}	40		45		ns
$t_{c(PM)}$	Page-mode read-modify-write cycle time	t_{PCM}	85		96		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	10		10		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 8)	t_{CAS}	15	10 000	18	10 000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge)	t_{RP}	40		50		ns
$t_{w(RL)}$	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RAS}	60	10 000	70	10 000	ns
$t_{w(RL)P}$	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RASP}	60	100 000	70	100 000	ns
$t_{w(WL)}$	Write pulse duration	t_{WP}	15		15		ns
$t_{su(CA)}$	Column-address setup time before $\overline{CAS}$ low	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time before $\overline{RAS}$ low	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time before $\overline{W}$ low (see Note 10)	t_{DS}	0		0		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low	t_{RCS}	0		0		ns
$t_{su(WCL)}$	$\overline{W}$-low setup time before $\overline{CAS}$ low (see Note 11)	t_{WCS}	0		0		ns
$t_{su(WCH)}$	$\overline{W}$-low setup time before $\overline{CAS}$ high	t_{CWL}	15		18		ns
$t_{su(WRH)}$	$\overline{W}$-low setup time before $\overline{RAS}$ high	t_{RWL}	15		18		ns
$t_{h(CA)}$	Column-address hold time after $\overline{RAS}$ low	t_{CAH}	10		15		ns
$t_{h(RA)}$	Row-address hold time after $\overline{RAS}$ low	t_{RAH}	10		10		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low (see Note 12)	t_{AR}	50		55		ns

Continued next page.

NOTES: 5. Timing measurements in this table are referenced to V_{IL} max and V_{IH} min.
6. All cycle times assume t_t = 5 ns.
7. To guarantee $t_{c(P)}$ min, $t_{su(CA)}$ should be greater than or equal to $t_{w(CH)}$.
8. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. (Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$)).
9. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. (Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$)).
10. Later of $\overline{CAS}$ or $\overline{W}$ in write operations.
11. Early write operation only.
12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

PARAMETER		ALT. SYMBOL	TMS44C256-80		TMS44C256-10		TMS44C256-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time (see Note 6)	t_{RC}	150		180		220		ns
$t_{c(W)}$	Write cycle time	t_{WC}	150		180		220		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	205		245		295		ns
$t_{c(P)}$	Page-mode read or write cycle time (see Note 7)	t_{PC}	50		55		65		ns
$t_{c(PM)}$	Page-mode read-modify-write cycle time	t_{PCM}	100		120		135		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	10		10		15		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 8)	t_{CAS}	20	10 000	25	10 000	30	10 000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge)	t_{RP}	60		70		90		ns
$t_{w(RL)}$	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RAS}	80	10 000	100	10 000	120	10 000	ns
$t_{w(RL)P}$	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RASP}	80	100 000	100	100 000	120	100 000	ns
$t_{w(WL)}$	Write pulse duration	t_{WP}	15		15		20		ns
$t_{su(CA)}$	Column-address setup time before $\overline{CAS}$ low	t_{ASC}	0		0		0		ns
$t_{su(RA)}$	Row-address setup time before $\overline{RAS}$ low	t_{ASR}	0		0		0		ns
$t_{su(D)}$	Data setup time before $\overline{W}$ low (see Note 10)	t_{DS}	0		0		0		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low	t_{RCS}	0		0		0		ns
$t_{su(WCL)}$	$\overline{W}$-low setup time before $\overline{CAS}$ low (see Note 11)	t_{WCS}	0		0		0		ns
$t_{su(WCH)}$	$\overline{W}$-low setup time before $\overline{CAS}$ high	t_{CWL}	20		25		30		ns
$t_{su(WRH)}$	$\overline{W}$-low setup time before $\overline{RAS}$ high	t_{RWL}	20		25		30		ns
$t_{h(CA)}$	Column-address hold time after $\overline{RAS}$ low	t_{CAH}	15		20		20		ns
$t_{h(RA)}$	Row-address hold time after $\overline{RAS}$ low	t_{RAH}	12		15		15		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low (see Note 12)	t_{AR}	80		70		80		ns

Continued next page.

NOTES: 5. Timing measurements in this table are referenced to V_{IL} max and V_{IH} min.
6. All cycle times assume t_t = 5 ns.
7. To guarantee $t_{c(P)}$ min, $t_{su(CA)}$ should be greater than or equal to $t_{w(CH)}$.
8. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. (Depending on the user's transition times, this may require additional $\overline{CAS}$ low time [$t_{w(CL)}$]).
9. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. (Depending on the user's transition times, this may require additional $\overline{RAS}$ low time [$t_{w(RL)}$]).
10. Later of $\overline{CAS}$ or $\overline{W}$ in write operations.
11. Early write operation only.
12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

	PARAMETER	ALT. SYMBOL	TMS44C256-60		TMS44C256-70		UNIT
			MIN	MAX	MIN	MAX	
$t_{h(D)}$	Data hold time after $\overline{CAS}$ low (see Note 10)	t_{DH}	10		15		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low (see Note 12)	t_{DHR}	50		55		ns
$t_{h(WLGL)}$	$\overline{G}$ hold time after $\overline{W}$ low	t_{GH}	15		18		ns
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ high (see Note 13)	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ high (see Note 13)	t_{RRH}	0		0		ns
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low (see Note 11)	t_{WCH}	15		15		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low (see Note 12)	t_{WCR}	50		55		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	60		70		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	15		18		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Note 14)	t_{CWD}	40		46		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 15)	t_{RCD}	20	45	20	52	ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column-address (see Note 15)	t_{RAD}	15	30	15	35	ns
$t_{d(CARH)}$	Delay time, column-address to $\overline{RAS}$ high	t_{RAL}	30		35		ns
$t_{d(CACH)}$	Delay time, column-address to $\overline{CAS}$ high	t_{CAL}	30		35		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 14)	t_{RWD}	85		98		ns
$t_{d(CAWL)}$	Delay time, column-address to $\overline{W}$ low (see Note 14)	t_{AWD}	55		63		ns
$t_{d(GHD)}$	Delay time, $\overline{G}$ high before data at DQ	t_{GDD}	15		18		ns
$t_{d(GLRH)}$	Delay time, $\overline{G}$ low to $\overline{RAS}$ high	t_{GSR}	10		10		ns
$t_{d(RLCH)R}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 16)	t_{CHR}	15		15		ns
$t_{d(CLRL)R}$	Delay time, $\overline{CAS}$ low $\overline{RAS}$ low (see Note 16)	t_{CSR}	10		10		ns
$t_{d(RHCL)R}$	Delay time, $\overline{RAS}$ high $\overline{CAS}$ low (see Note 16)	t_{RPC}	0		0		ns
t_{rf}	Refresh time interval	t_{REF}		8		8	ms
t_t	Transition time	t_T	3	50	3	50	ns

Continued next page.

NOTES: 5. Timing measurements in this table are referenced to V_{IL} max and V_{IH} min.
10. Later of $\overline{CAS}$ or $\overline{W}$ in write operations.
11. Early write operation only.
12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
13. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.
14. Read-modify-write operation only.
15. Maximum value specified only to guarantee access time.
16. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

PARAMETER		ALT. SYMBOL	TMS44C256-80		TMS44C256-10		TMS44C256-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{h(D)}$	Data hold time after $\overline{CAS}$ low (see Note 10)	t_{DH}	15		20		25		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low (see Note 12)	t_{DHR}	60		70		85		ns
$t_{h(WLGL)}$	$\overline{G}$ hold time after $\overline{W}$ low	t_{GH}	20		25		30		ns
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ high (see Note 13)	t_{RCH}	0		0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ high (see Note 13)	t_{RRH}	0		0		0		ns
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low (see Note 11)	t_{WCH}	15		20		25		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low (see Note 12)	t_{WCR}	60		70		85		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	80		100		120		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	20		25		30		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Note 14)	t_{CWD}	50		60		70		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 15)	t_{RCD}	22	60	25	75	25	90	ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column-address (see Note 15)	t_{RAD}	17	40	20	55	20	65	ns
$t_{d(CARH)}$	Delay time, column-address to $\overline{RAS}$ high	t_{RAL}	40		45		55		ns
$t_{d(CACH)}$	Delay time, column-address to $\overline{CAS}$ high	t_{CAL}	40		45		55		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 14)	t_{RWD}	110		135		160		ns
$t_{d(CAWL)}$	Delay time, column-address to $\overline{W}$ low (see Note 14)	t_{AWD}	70		80		95		ns
$t_{d(GHD)}$	Delay time, $\overline{G}$ high before data at DQ	t_{GDD}	20		25		30		ns
$t_{d(GLRH)}$	Delay time, $\overline{G}$ low to $\overline{RAS}$ high	t_{GSR}	10		10		10		ns
$t_{d(RLCH)R}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 16)	t_{CHR}	20		25		25		ns
$t_{d(CLRL)R}$	Delay time, $\overline{CAS}$ low $\overline{RAS}$ low (see Note 16)	t_{CSR}	10		10		10		ns
$t_{d(RHCL)R}$	Delay time, $\overline{RAS}$ high $\overline{CAS}$ low (see Note 16)	t_{RPC}	0		0		0		ns
t_{rf}	Refresh time interval	t_{REF}		8		8		8	ms
t_t	Transition time	t_T	3	50	3	50	3	50	ns

NOTES: 5. Timing measurements in this table are referenced to V_{IL} max and V_{IH} min.
10. Later of $\overline{CAS}$ or $\overline{W}$ in write operations
11. Early write operation only.
12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
13. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle
14. Read-modify-write operation only.
15. Maximum value specified only to guarantee access time
16. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.

PARAMETER MEASUREMENT INFORMATION

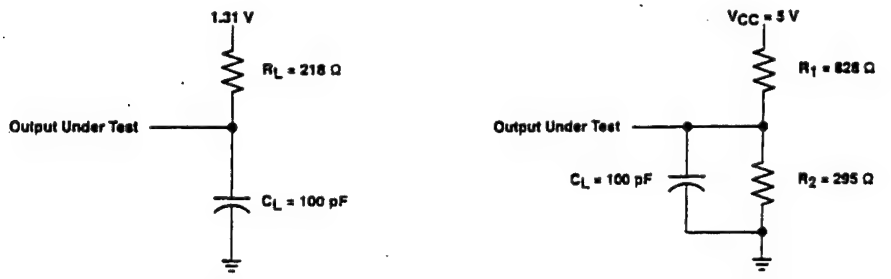
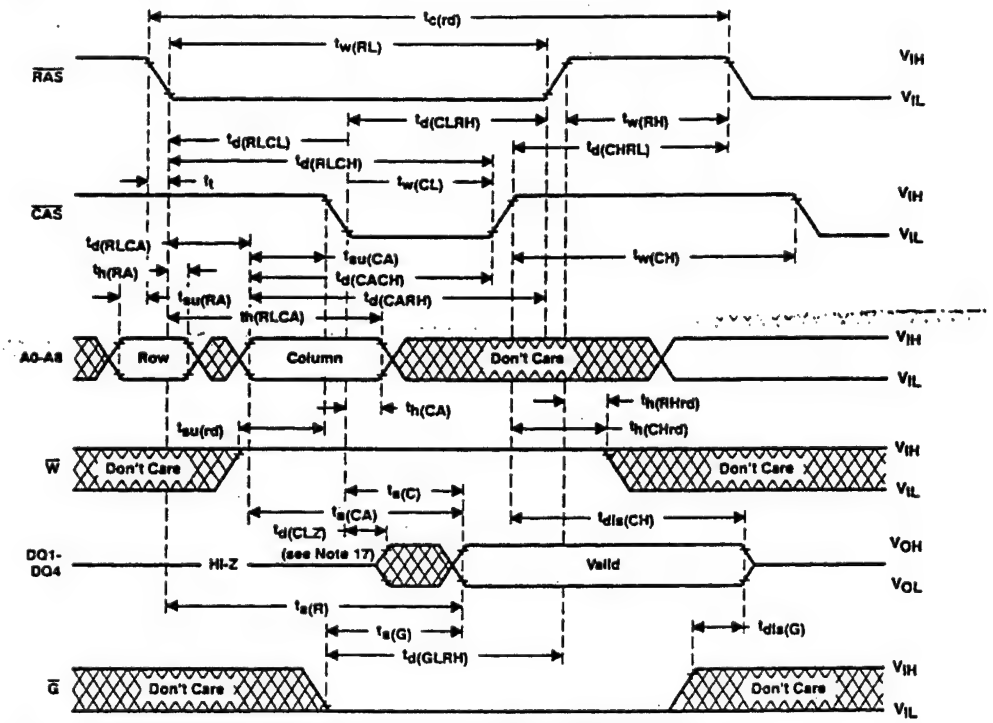


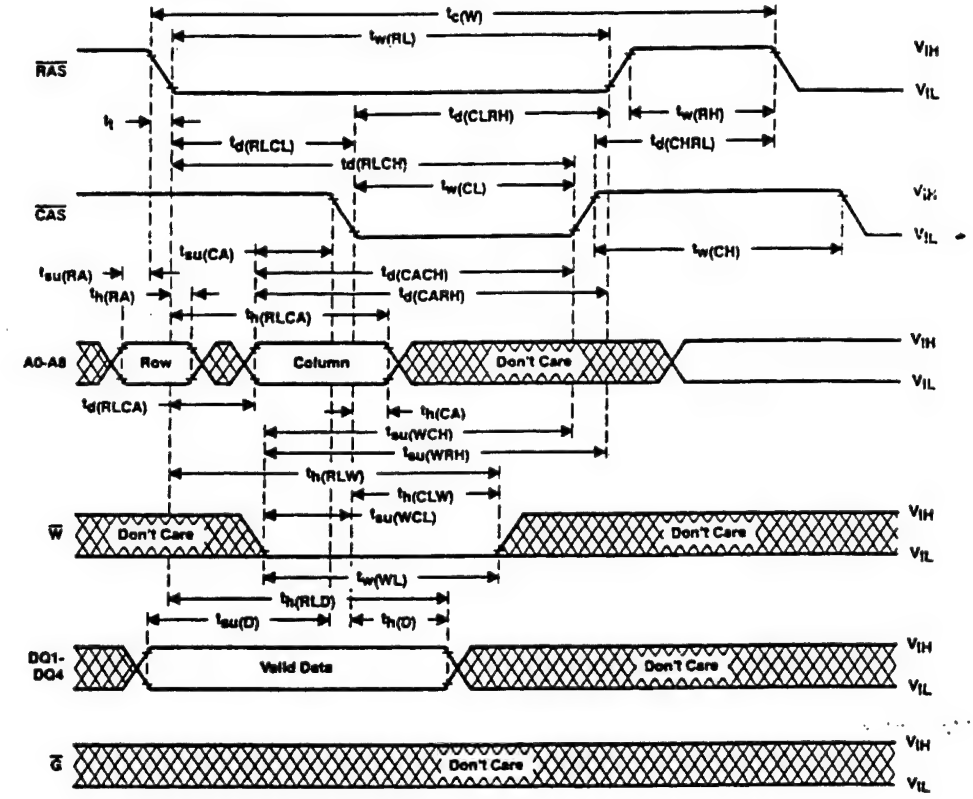
Figure 1. Load Circuits for Timing Parameters

read cycle timing

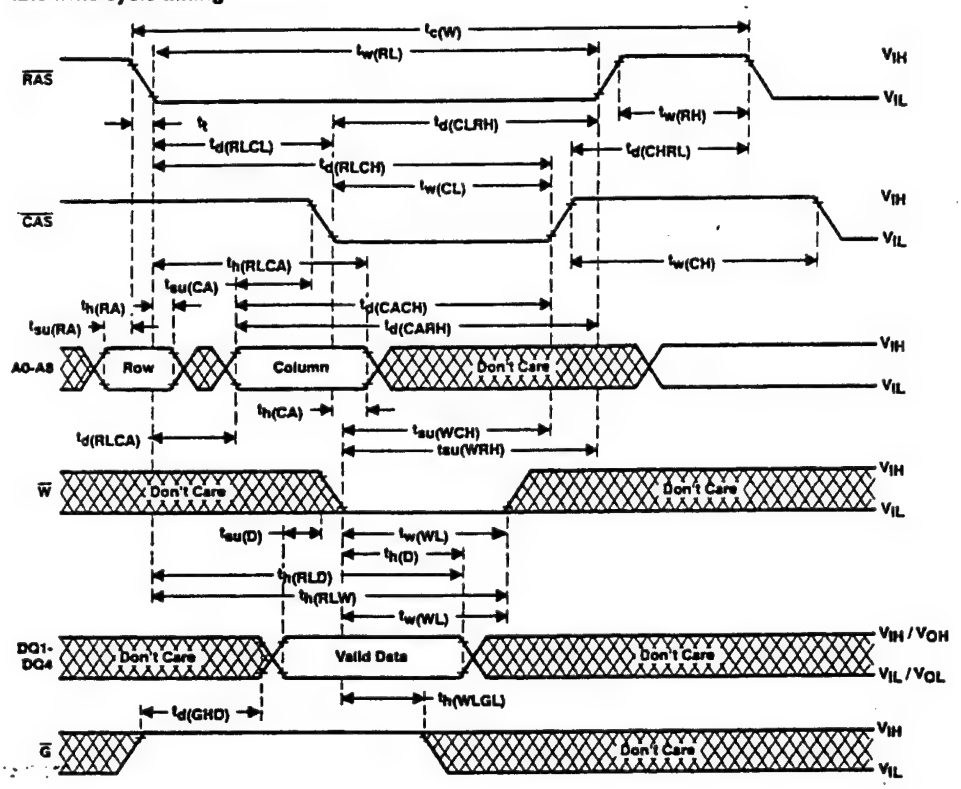


NOTE 17: Output may go from high-impedance to an invalid data state prior to the specified access time.

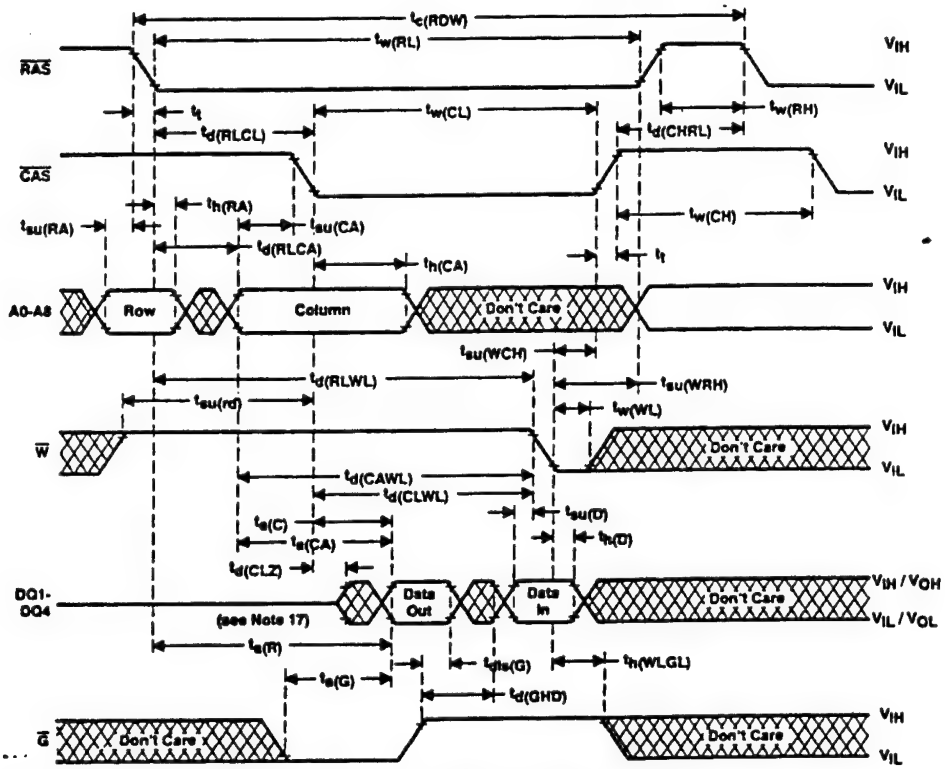
early write cycle timing



late write cycle timing

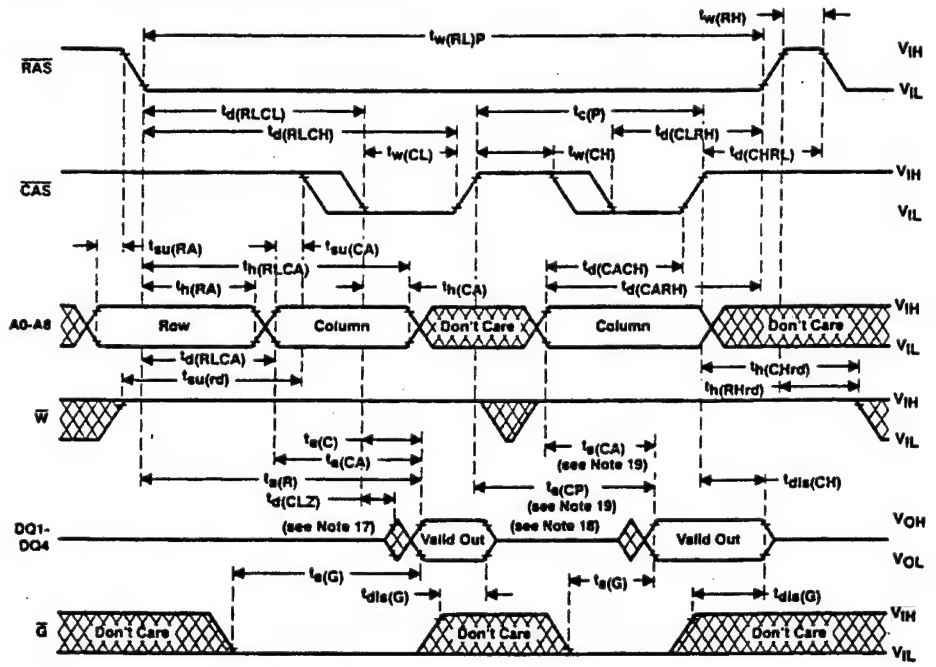


read-write/read-modify-write cycle timing



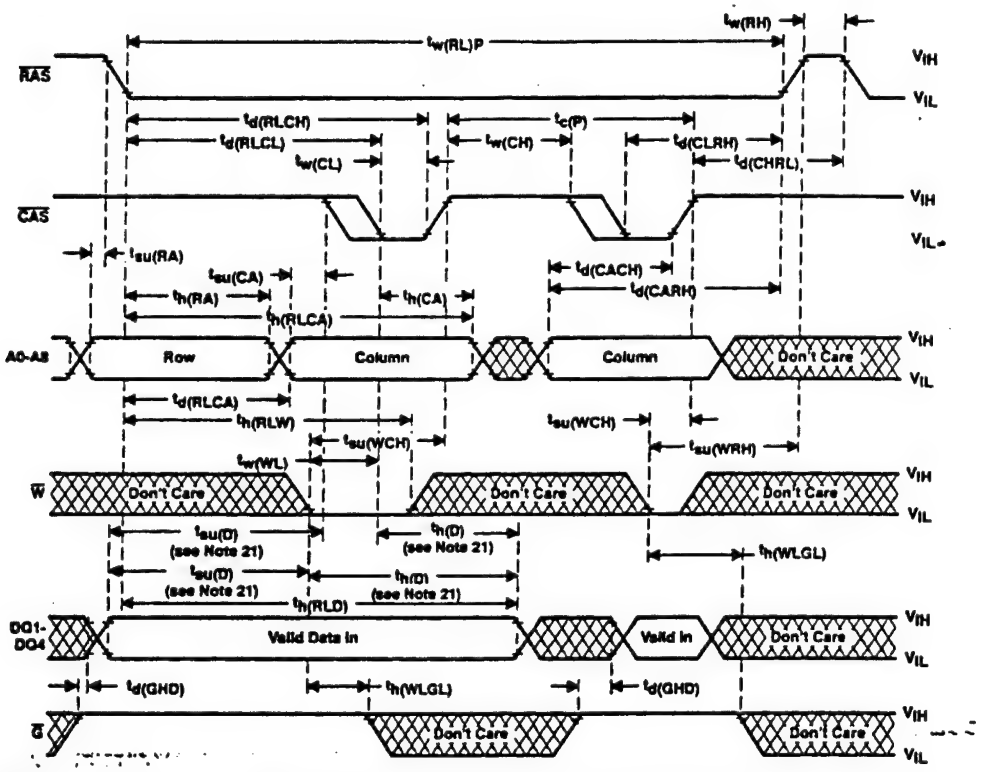
NOTE 17: Output may go from high-impedance to an invalid data state prior to the specified access time.

enhanced page-mode read cycle timing



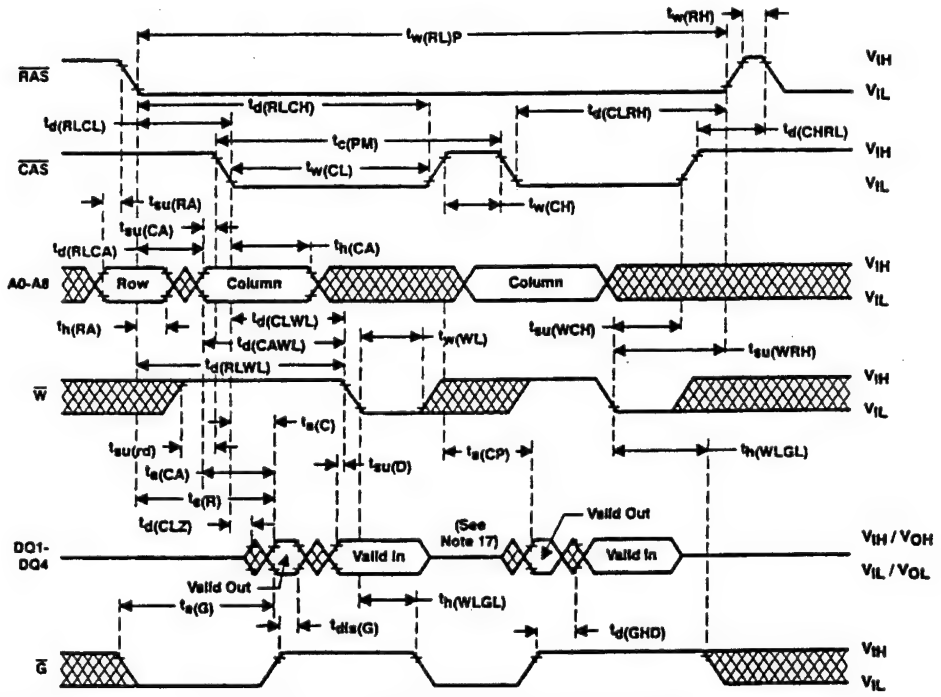
NOTES: 17. Output may go from high-impedance to an invalid data state prior to the specified access time.
18. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.
19. Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.

enhanced page-mode write cycle timing



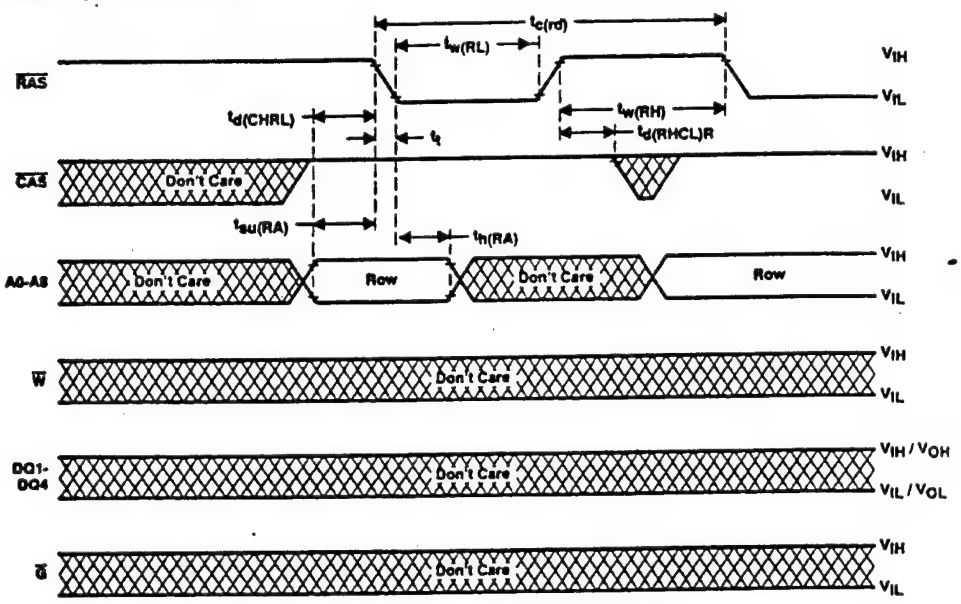
NOTES: 20. A read cycle or a read-modify-write cycle can be intermixed with the write cycles as long as the read and read-modify-write timing specifications are not violated.
21. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.

enhanced page-mode read-modify-write cycle timing

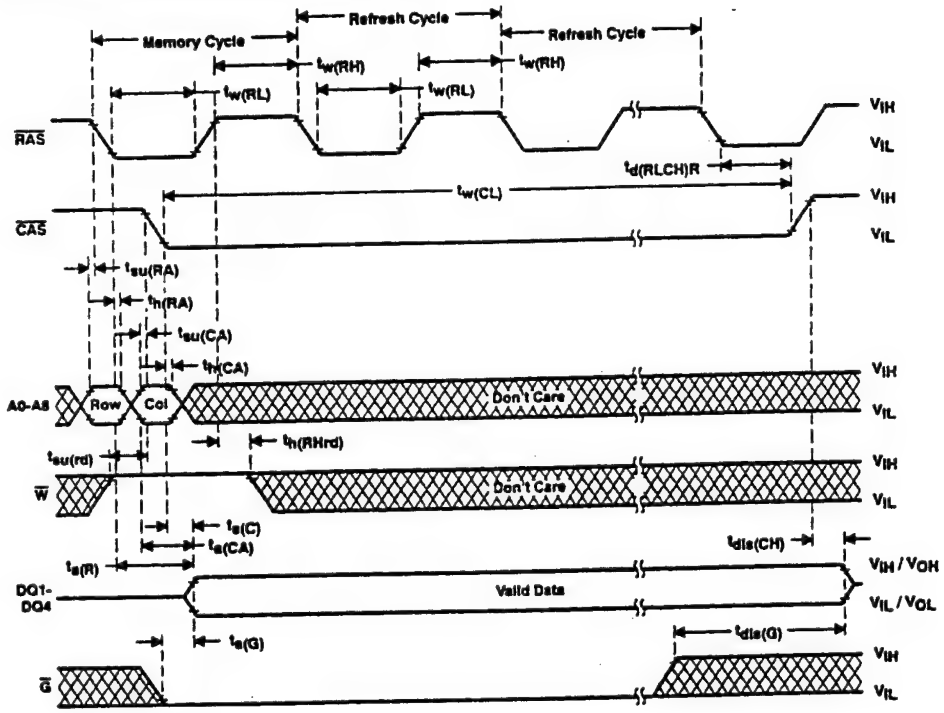


NOTES: 17. Output may go from high-impedance to an invalid data state prior to the specified access time.
22. A read or write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

$\overline{RAS}$-only refresh timing



hidden refresh cycle (enhanced page mode)



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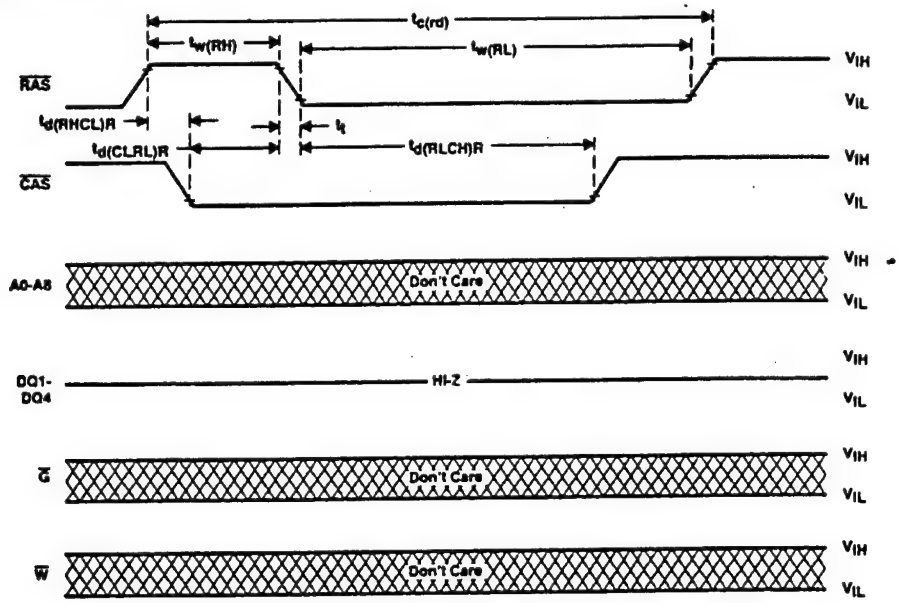
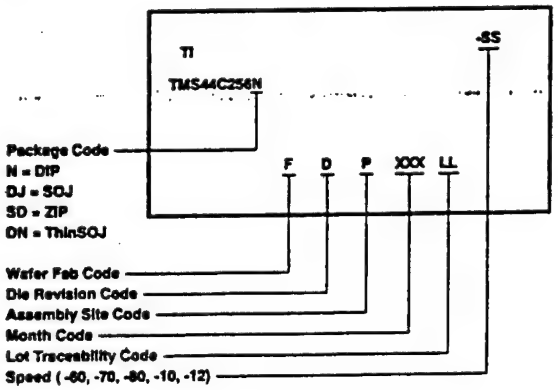
automatic ($\overline{CAS}$-before-$\overline{RAS}$) refresh cycle timing



device symbolization



MOS Memory

DRAMs and VRAMs

Introduction

TI's military DRAM family includes a broad selection of devices for high-density memory design. Ranging from 64K-bit to 4M-bit densities, TI's military DRAMs are available in several output configurations and organizations, package options, temperature, and speed performance ranges to meet your military system requirements.

The 256K DRAMs provide upward pin compatibility from the 64K DRAMs. Access times from row address strobe for these two densities are 120, 150, and 200 ns, with a 256-row 4-ms refresh cycle.

The high-speed 1M and 4M DRAMs utilize state-of-the-art EPIC™ (Enhanced-Performance Implanted CMOS) technology for high performance, reliability, and low power at a low cost. This EPIC™ technology permits operation from a single 5-V supply, reducing system power supply and decoupling requirements and easing board layout.

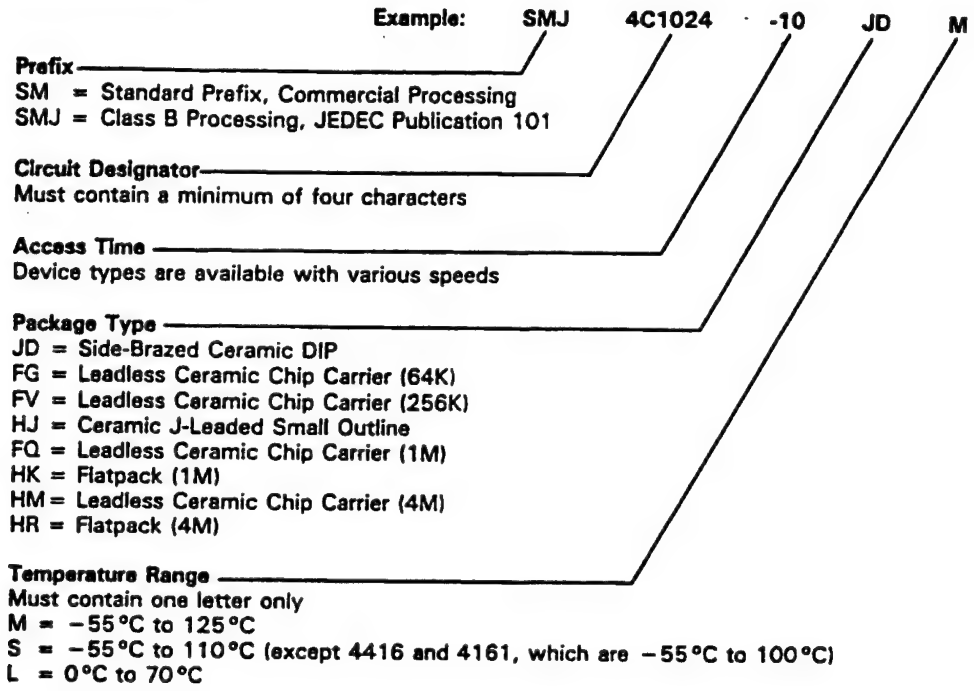
As the product density increases, product performance is improved. Beginning at the 1M density, the use of CMOS technology provides the benefits of faster access times and lower power dissipation. Another benefit of CMOS technology is that it allows operation over the full military temperature range, −55°C to 125°C, which is an increase from the −55°C to 110°C operation of NMOS Dynamic RAMs.

An important area of performance improvement for the 1M-bit DRAM and beyond is the offering of enhanced page-mode operation. Page-mode operation allows faster access by keeping the same row address while selecting random column addresses. Unlike page-mode, enhanced page-mode allows the column address decode and, therefore, data retrieval to begin prior to the falling edge of $\overline{CAS}$. This allows the memory system to operate at a higher data bandwidth than conventional page-mode devices.

Texas Instruments offers a complete line of video memory products. Currently available are the SMJ4161 (64K × 1) video RAM with separate serial-in and serial-out ports, and the SMJ4461 (64K × 4) video RAM with 22-MHz serial-port shift rates. Texas Instruments is continuing its pursuit of high-density, high-speed video RAMs with the militarization of the SMJ44C250 and SMJ44C251 1M-bit video RAM. The SMJ44C251 CMOS device offers numerous special features such as enhanced page-mode, 4 × 4 block write, write-per-bit for selective writes to each RAM I/O, 512-tap serial data registers, color register, masking features, and split-register transfers. TI's video RAM is a perfect match for the 340 graphics family processors.

EPIC is a trademark of Texas Instruments Incorporated.

Nomenclature



3-4

Product Spectrum

DEVICE	TEMP	TYPE	MAX ACCESS TIME (ns) (FROM ROW STROBE)	‡PACKAGE TYPE (NO. OF PINS)							
				JD	FG	FV	HJ	FQ	HK	HR	HM
4164	S	DRAM	120/150/200	16	18						
4256	S	DRAM	120/150/200	16		18					
4464	S	DRAM	120/150/200	18							
4C1024	M	DRAM	90†/100/120/150	18			20	20	20		
44C256	M	DRAM	100/120/150	20			20†	20			
44100†	M	DRAM	80/100/120	18						20	20
44400†	M	DRAM	80/100/120	20						20	20
4461	S	VRAM	120/150	24							
44C250†	M	VRAM	120	28			28				
44C251†	M	VRAM	120	28			28				

†Planned product. Contact factory for release dates.
‡Package type
JD = Side-Brazed Ceramic DIP
FG = Leadless Ceramic Chip Carrier (64K)
FV = Leadless Ceramic Chip Carrier (256K)
HJ = Ceramic J-Leaded Small Outline (1M)
FQ = Leadless Ceramic Chip Carrier (1M)
HK = Flatpack (1M)
HM = Leadless Ceramic Chip Carrier (4M)
HR = Flatpack (4M)

Cross-Reference

COMPANY	NOMENCLATURE
TI	SMJ XXXX-XXYYX
MICRON	MT XXXXYY-XX 883C

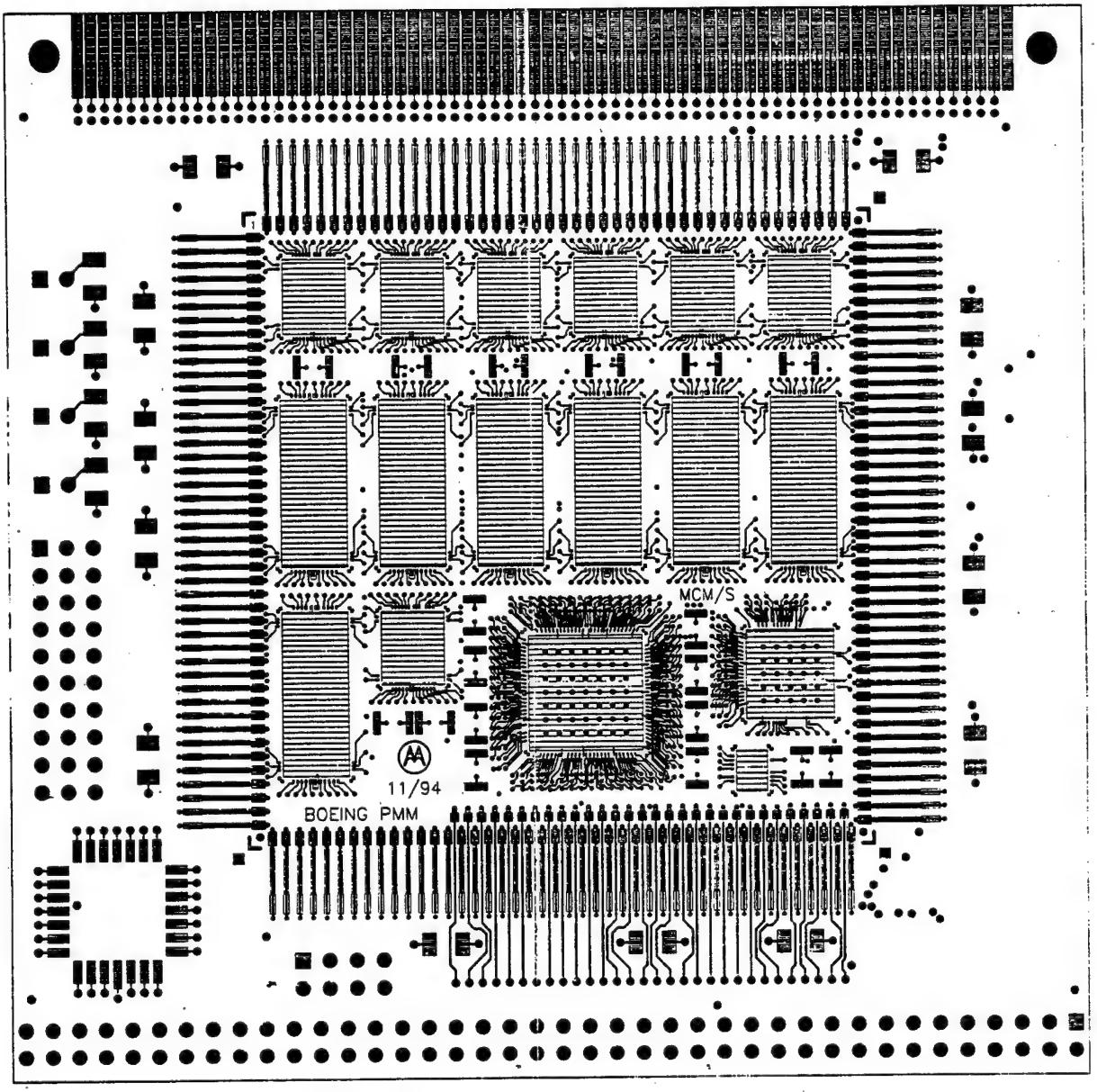
EPROMs

Introduction

TI's military memory offering also includes a full family of high-density CMOS UV EPROMs designed to meet your system requirements.These ultraviolet-light-erasable, electrically programmable read-only memories are available in densities of 128K bits, 256K bits, and 512K bits, with a future release of a 1M-bit device planned. Enhanced-speed versions of the 128K-bit and 256K-bit EPROMs are available to provide reduced-wait-state operation for today's high-speed processors.

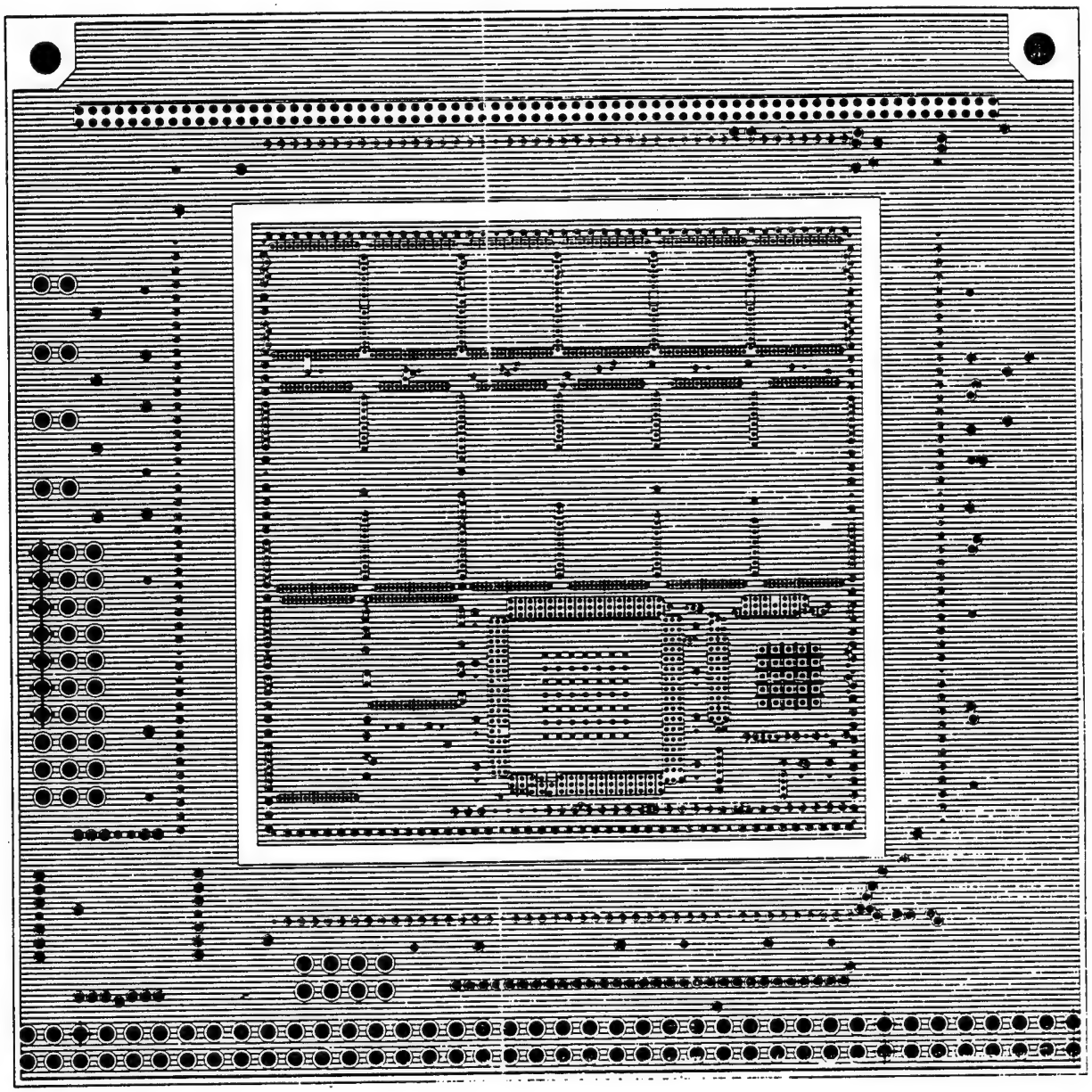
The SMJ27C128, SMJ27C256, and SMJ27C512 are fabricated using HVCMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including data inputs during programming) can be driven by Series 54 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 54 TTL circuit without external pull-up resistors. The data outputs provide three-state operation for connecting multiple devices to a common bus.

Appendix B –Photo-Plot Images of PMM Laminated Substrate



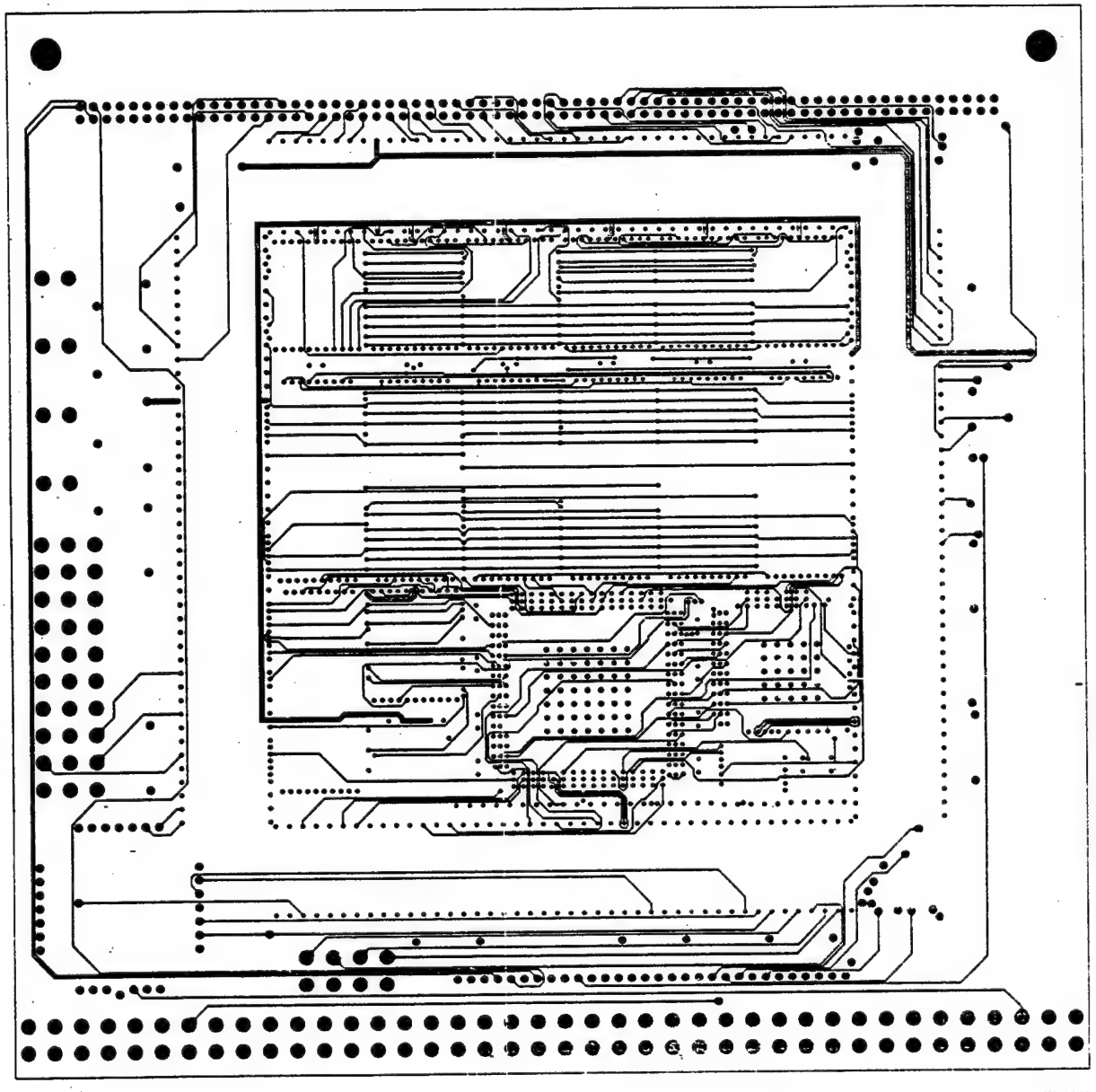
LAYER 1 TOP

Appendix B –Photo-Plot Images of PMM Laminated Substrate



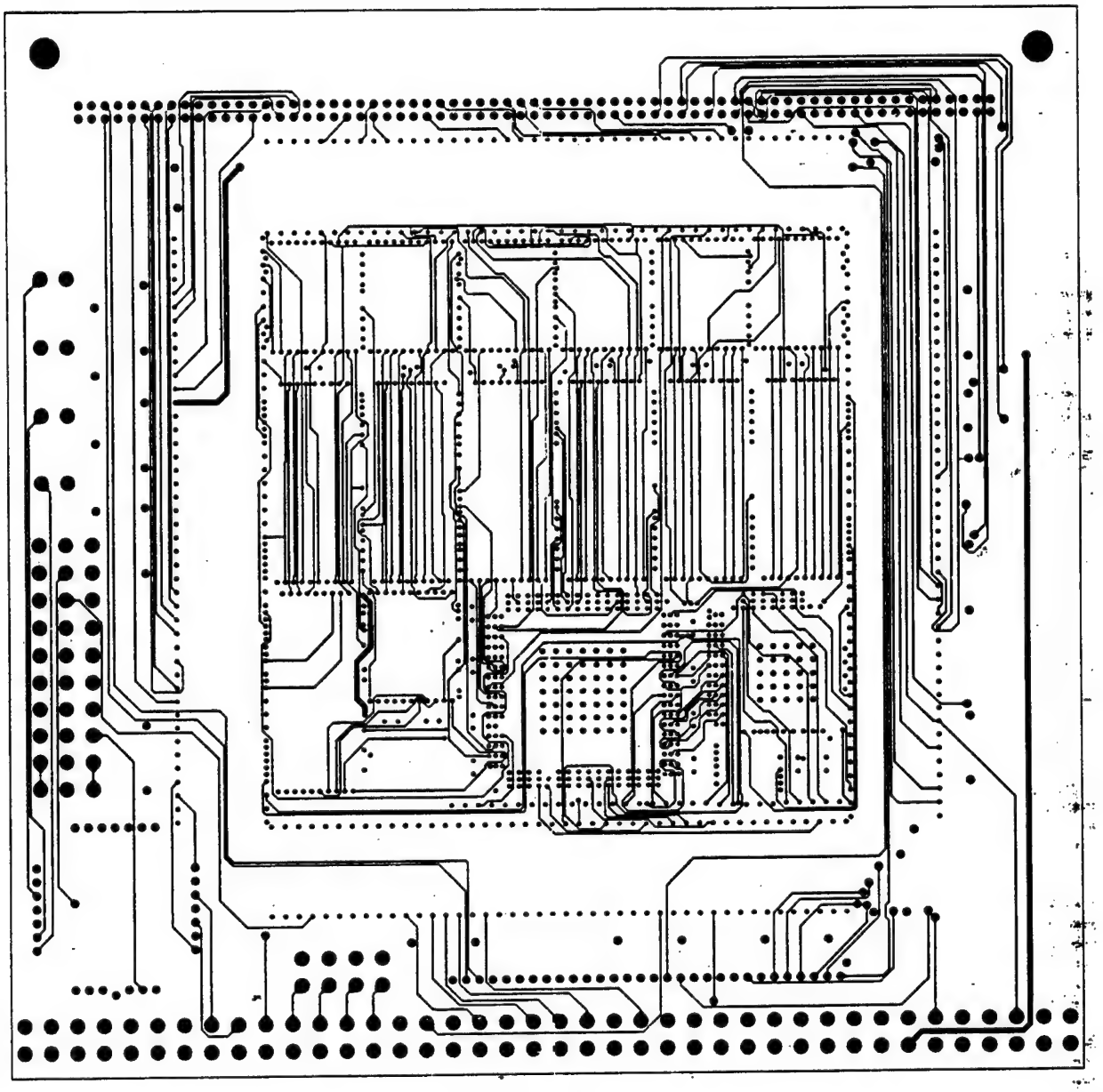
LAYER 2

Appendix B –Photo-Plot Images of PMM Laminated Substrate



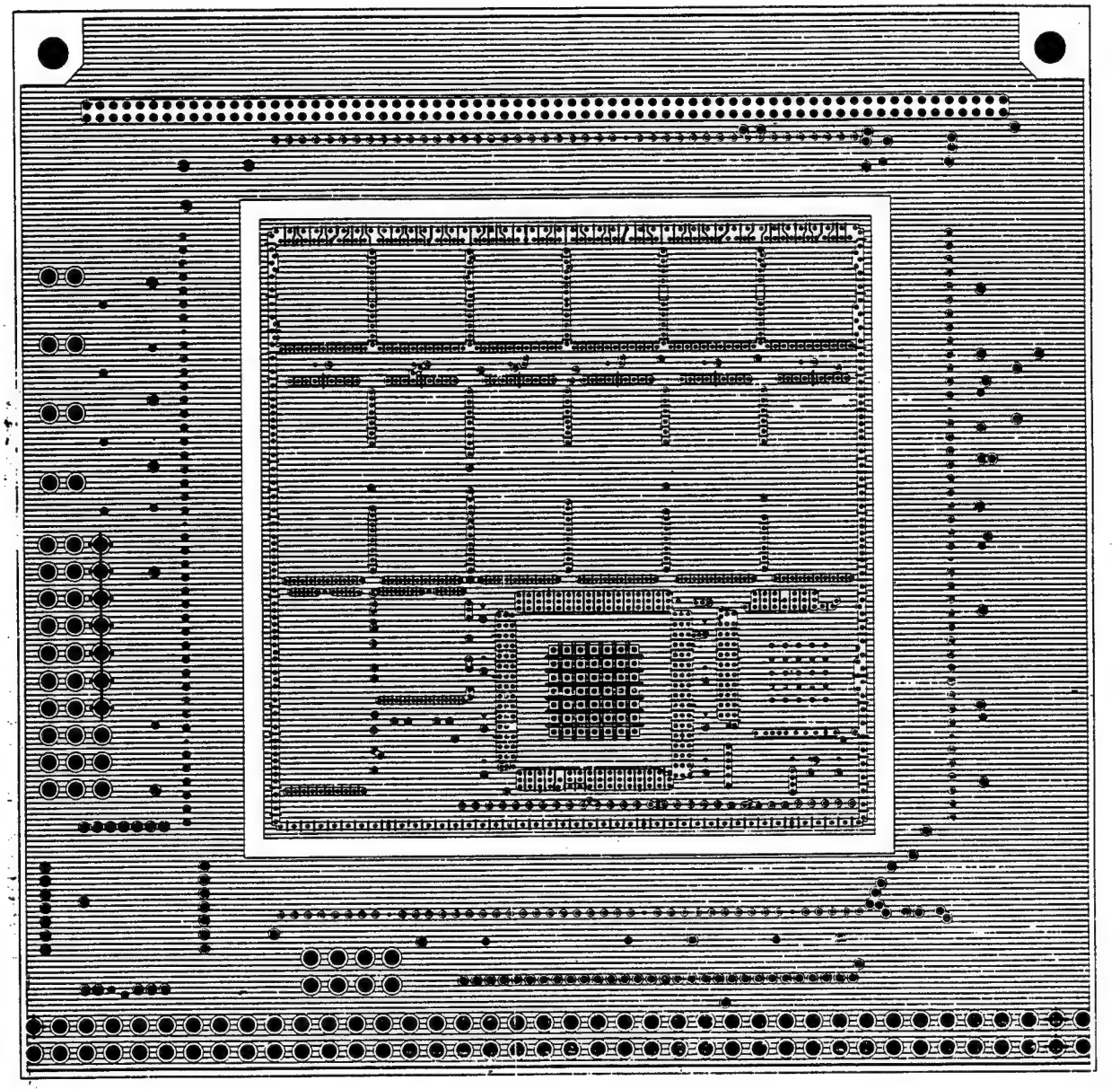
LAYER 3

Appendix B –Photo-Plot Images of PMM Laminated Substrate



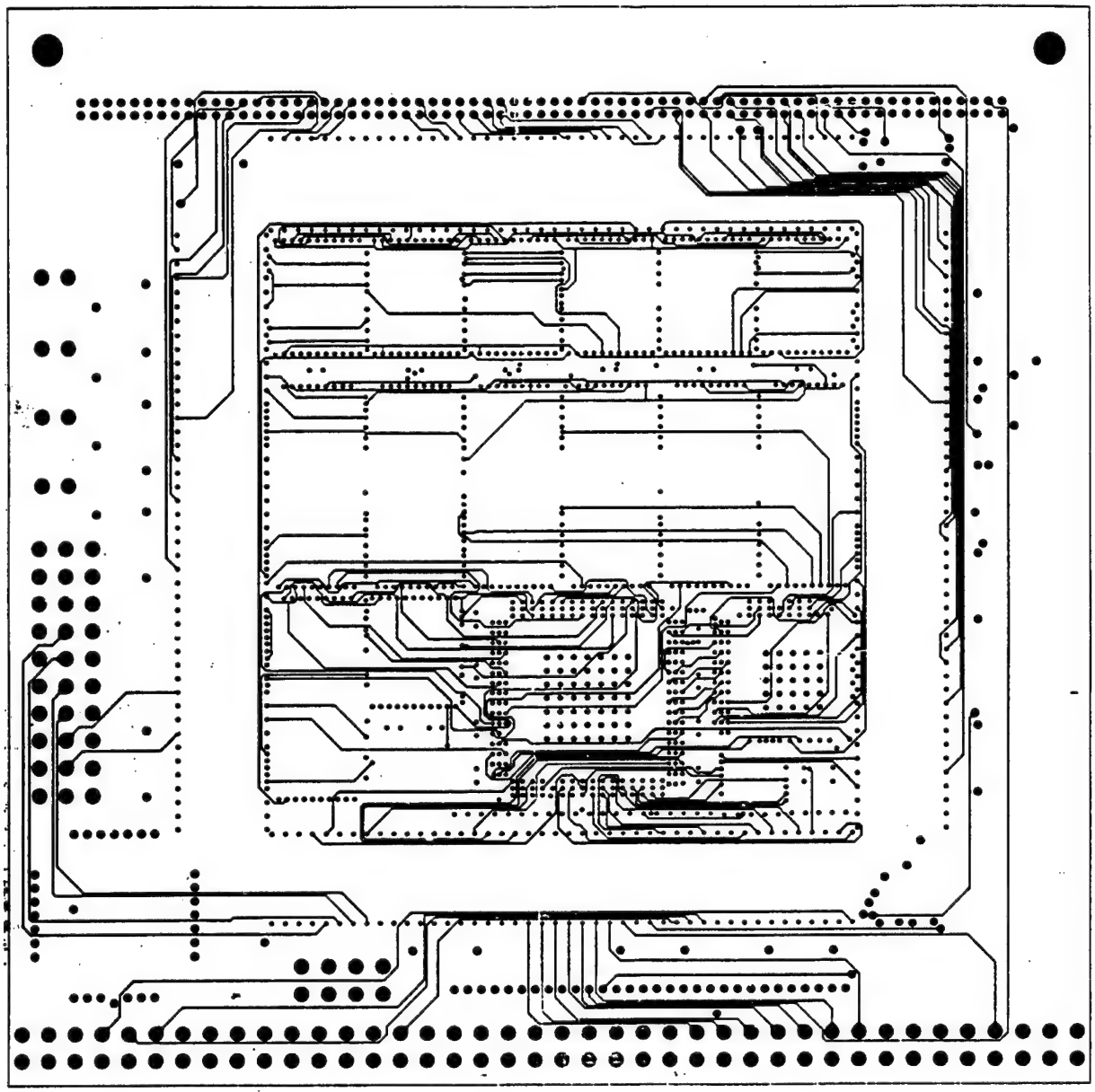
LAYER 4

Appendix B –Photo-Plot Images of PMM Laminated Substrate



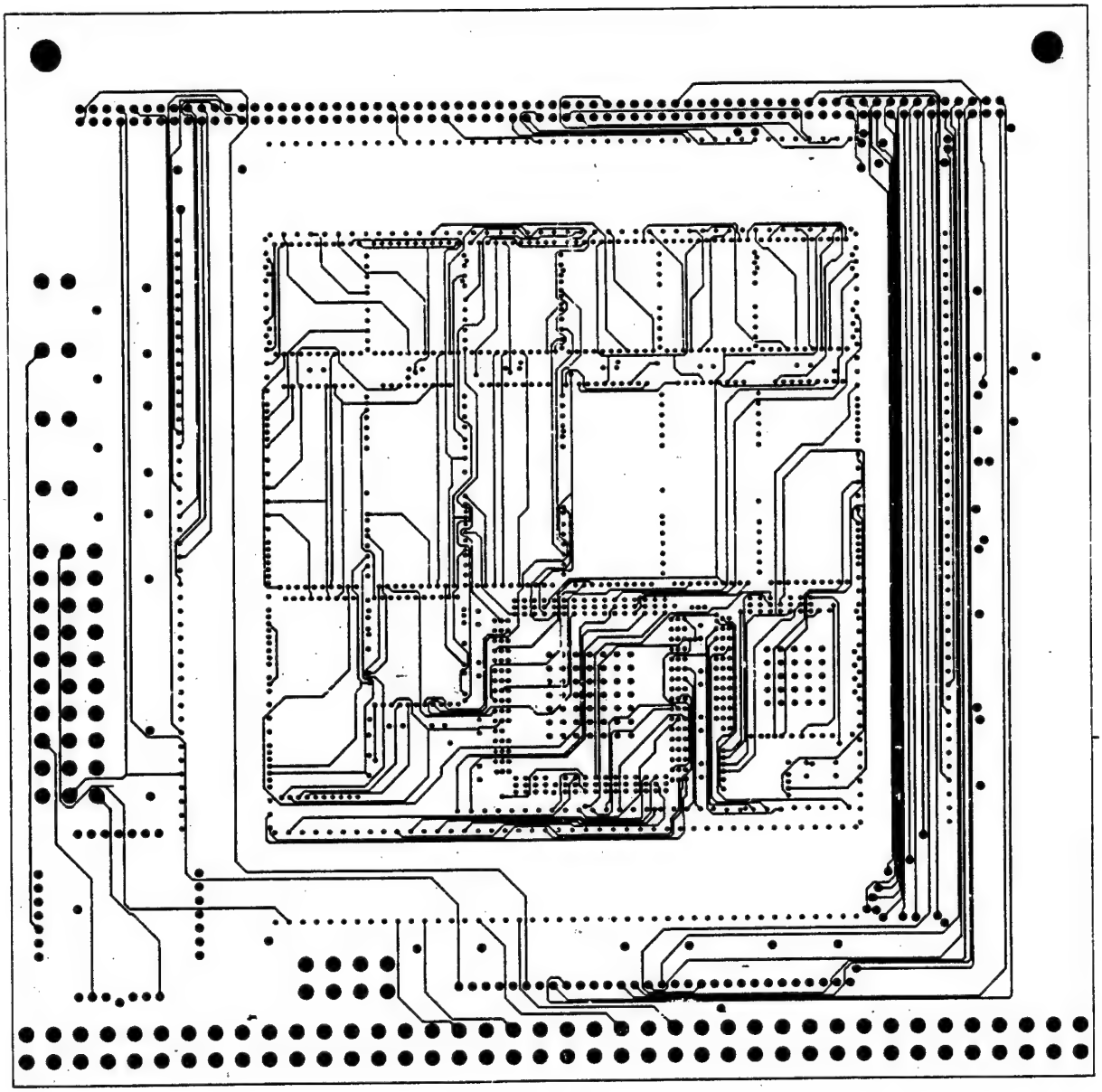
LAYER 5

Appendix B –Photo-Plot Images of PMM Laminated Substrate



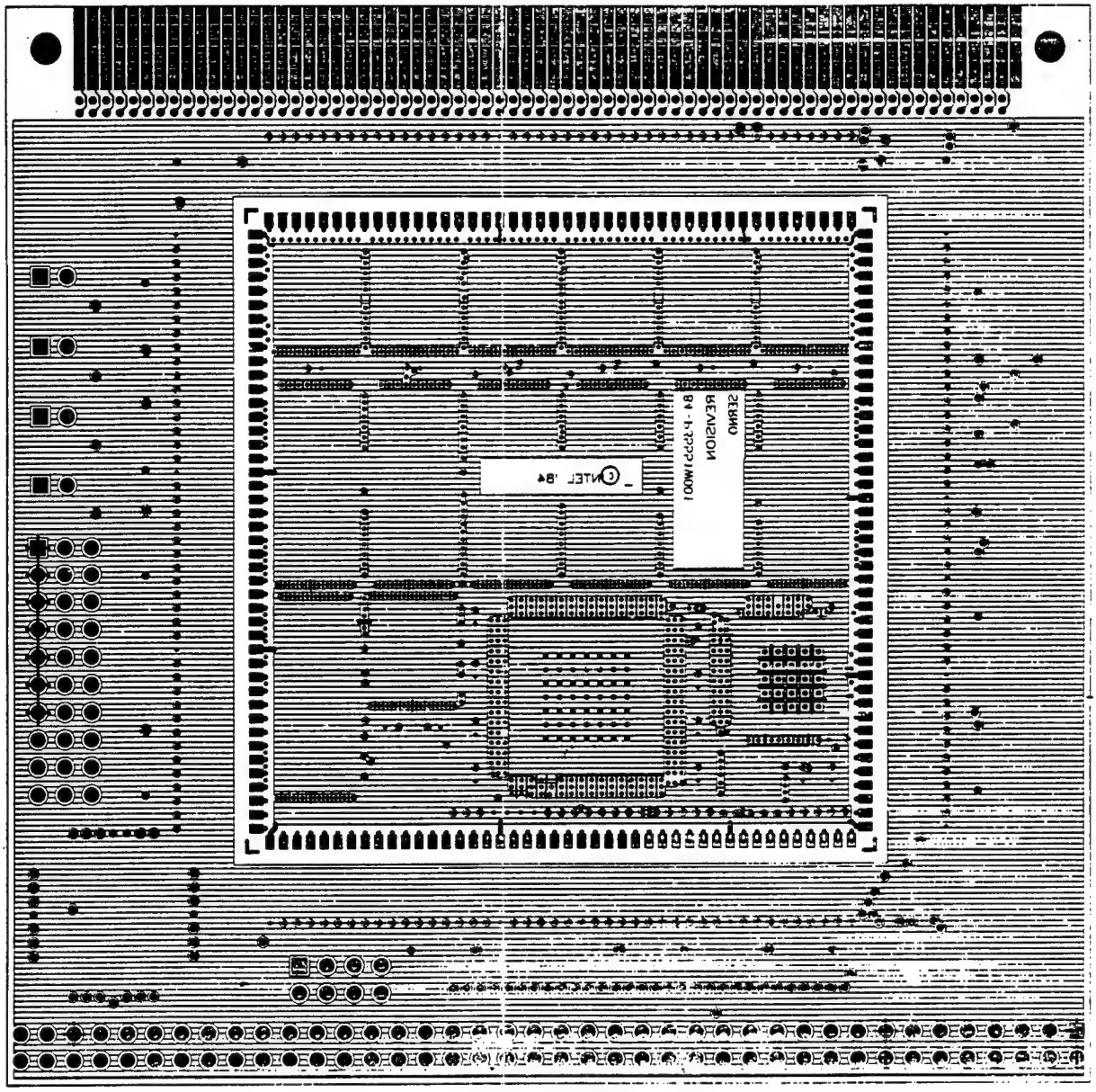
LAYER 6

Appendix B –Photo-Plot Images of PMM Laminated Substrate



LAYER 7

Appendix B –Photo-Plot Images of PMM Laminated Substrate



LAYER 8 BOTTOM

Appendix C: Operators Instruction for EMEAP Test Fixture

The purpose of this instruction is to assist the test operator a) to identify the individual parts that make up this test fixture, b) to understand how to prepare the fixture for use, and c) to perform conducted susceptibility testing on a number of different test devices using the test fixture. The two test devices that are specifically addressed are the 3DMM and PMM. Test fixture set-up for other analog or digital electronic devices can be accomplished by modifying these instructions as needed.

List of parts:

- Test Fixture (includes 1 cable between top and bottom boards)
- Top & Bottom Adapter Set #1 (includes 2 cables per fixture)
- Top & Bottom Adapter Set #2 (includes 4 cables per fixture)
- Top & Bottom Adapter Set #3 (includes 2 cables per fixture)
- Top & Bottom Adapter Set #4
- Through-Signal Adapters (40)
- Diplexer Signal Combiners (6)
- High Speed Op-Amp Signal Combiners (9)
- High Power Op-Amp Signal Combiners (7)
- Diplexer + Wide-band Amp Signal Combiners, 500 MHz – 2 GHz, 1 Watt (4)
- Diplexer + Wide-band Amp Signal Combiners, 2 GHz to 6 GHz, 2 Watt (2)
- Diplexer + Wide-band Amp Signal Combiners, 2 GHz to 8 Ghz, 1 Watt
- Diplexer + Wide-band Amp Signal Combiners, 6 to 18 GHz, 1 Watt, 2 (2)
- Edge board extender, 140 pin
- 3DMM connector adapters (2)
- Signal combiner hold down screws (80+)

Identifying Marks:

- The test fixture has an arrow on top of the top circuit board near one of the access holes. This arrow indicates the orientation of pin 1 for both the 3DMM and PMM test devices.
- The top adapters and bottom adapters have pin "1" identified for use in orienting them in the same direction as the test fixture.
- The 3DMM has different color glass seals around the pins. The white glass seal is pin 1. Pin 13, which is Vss or ground, is connected directly to the case and has no glass seal. Pins 2 through 12 and 14 through 50 have green glass seals.
- When looking at the component side of the PMM with the 140 pin edge connector facing down, pin 1 is the left most contact of the edge connector and pin 70 is the right most pin. Pin 71 is directly behind pin 70 on the back side of the board and pin 140 is directly behind pin 1.

Use of Signal Combiners in EMEAP Test Fixture:

- Insert all 40 of the through signal adapters into the sockets in the side of the test fixture to run signals straight from the input connector (bottom) through to the device-under-test connector (top) of the test fixture. The RF connectors will usually hold these adapters in place for short tests, but we would recommend using at least the top hold-down screw to hold the combiners securely against the test fixture.
- When using the high-speed op-amp combiner, high-power op-amp combiner, or the diplexer/wide-band amp combiner, DC power must be supplied to the test fixture. The red jack is plus 15V, blue is negative 15 V, and black is common. We would recommend that the power supplies be left floating

(not grounded) and that the ground reference be established through the RF instrumentation. We would also recommend the use of power supplies with a current rating of at least 10 amps.

- When installing any of the DC powered combiners mentioned above, engage the DC contacts before attempting to push in the RF contacts. You should use at least the top hold-down screw to hold the combiners securely against the test fixture.
- The diplexer signal combiners are designed to work over a frequency range from about 500 KHz to nearly 18 GHz, but each one does has unique RF characteristics. See Figures 1 through 6 for the diplexer characteristics between 500 MHz and 20 GHz and Figures 7 and 8 for the low frequency characteristics of diplexers 1-1 and 2-7.
- Figure 9 gives the characteristics of the different types of wideband amplifiers. Figure 10 gives the gain through the different wideband-amplifier/diplexer signal combiners so that the RF gain through the interfering signal leg can be calculated at whatever frequency is being used.
- The frequency range of the interfering signal for the high-speed op-amp combiner is 1 KHz to approximately 170 MHz. Several of these combiners have 50 ohm matching resistors at the interfering signal input for good match, but the maximum power input for these is about 1 watt. Several of these combiners have 200 ohm matching resistors at the interfering signal input for a near match but up to +/- 8V signal input.
- The frequency range of the interfering signal for the high-power op-amp combiner is 1 Hz to approximately 90 MHz. Several of these combiners have 50 ohm matching resistors at the interfering signal input for good match, but the maximum power input for these is about 1 watt. Several of these combiners have 200 ohm matching resistors at the interfering signal input for a near match but up to +/- 10V signal input.
-

Test fixture setup - 3DMMM:

1. Use the arrow on the test fixture top board to indicate pin 1 of the 3DMM. Plug the 3DMM into the test fixture with pin1 next to the arrow. The cable coming from the automated tester should also be oriented so that it's pin 1 matches that of the test fixture. The major identifying marks on the 3DMM are the white glass seal on pin 1 and no glass seal on pin 13. The rest of the pins have green glass seals. Because the 3DMM has 50 pins and the interface connector on the EMEAP test fixture has 62 pins, it is possible to insert the 3DMM a number of different ways.
2. Install the 3DMM in the test fixture so that Pin 1 is on the side of the test fixture that is closest to the arrow near one of the connector access holes. Because the connector interface has 62 pins and the 3DMM has only 50 it is possible to insert it in the test fixture a number of ways. We suggest that only two positions be used for the 3DMM – all the way to the right in the test fixture and all the way to the left. By using only these two positions you will be able to test all of the 49 signals and voltages of the 3DMM on the 40 signal test fixture. The 3DMM signals that do not travel through one of the 40 signal sites of the test fixture are transferred between top and bottom test fixture signals layers via a bypass cable. The pin numbers, their corresponding signal name, and signal location on the test fixture for the two orientations of the 3DMM, are shown in Figure 11.
3. Insert the 2 - 3DMM cable adapters into the connector from the automated tester. Insert the cable/adapter from the automated tester into the connector on the bottom board to exactly duplicate the position of the 3DMM.
4. The 3DMM should now be ready to test. The cable from the automated tester also includes Vcc and ground.

Appendix C: Operators Instruction for EMEAP Test Fixture

Test fixture setup - PMM:

1. The PMM has two power supply inputs, Vdd (power supply) and Vpp (programming voltage), which must be connected correctly or the test devices may be damaged or destroyed. The two power supply pins are on the non-component (back) side of the PMM. With the 140 pin edge connector facing down, looking at the back side of the board, the Vdd pin on the PMM is the right pin (pin 42) and the Programming Voltage pin is the left pin (pin 47). They are on the 80-pin connector pattern on the top of the PMM, and pin 1 is the square pad.
2. Locate the signal pins on the PMM as follows: When looking at the component side of the PMM with the 140 pin edge connector facing down pin 1 is the left most contact of the edge connector and pin 70 is the right most pin. Pin 71 is directly behind pin 70 on the back side of the board and pin 140 is directly behind pin 1. It is convenient to use the arrow on the test fixture top to indicate pin 1 of the PMM. The cable coming from the automated tester should also be oriented so that it's pin 1 matches pin 1 of the test fixture.
3. Insert the PMM into the top adapter socket so that pin 1 is next to the "1" silk-screened on the board. Install the bypass cables on the top adapter before installing it into the top of the test fixture.
5. To install one of the PMM adapter sets into the EMEAP test fixture position the adapter, with the cables attached to the top adapter, so that the cables hang through the connector access hole(s). Insert the adapter pins into the center portion of the 62 pin socket so that there are 3 spare sockets left in each outside row. Turn the test fixture onto it's top, position the matching bottom adapter next to the bottom test fixture connector and plug in the bypass cables. Insert the bottom adapter into the bottom 62 pin connector, observing to leave 3 spare sockets in each outside row just like with the top adapter. The pin numbers, their corresponding signal name, and signal location on the test fixture for the three orientations of the PMM, are shown in Figures 12A through 12D.
4. Turn the test fixture and place it upright. Locate pin 1 on the 140 pin connector coming from the automated tester. Insert a 140 pin board edge extender into the connector. Position the test fixture over the automated tester and plug the connector/extender into the bottom connector of the test fixture observing a pin1 to pin1 orientation.
6. Connect Vcc from the automated tester to the Vcc pin on the PMM. Connect the programming voltage clip from the automated tester to the programming voltage pin on the PMM.
7. The test fixture is now ready to test the PMM.

Test planning

1. Set up the test fixture with all 40 of the through-signal adapters installed. Attach it to the test signal source, which will generally be an automated test system. Make sure the cable is oriented properly with respect to the intended location of the device under test.
2. Insert the test device. Run the test program to successful completion to ensure the test system and test fixture are properly configured.
3. Determine which signals in the test device are to receive an interfering signal and set up test parameters. Determine approximate susceptibility level for the test, then begin the test at a power level somewhat below the susceptibility level.
4. Remove the through-signal adapter and install the appropriate signal combiner in the test slot designated for the test. Connect a signal source to the signal combiner. Energize DC power to the test fixture if required, and energize the signal source.
5. Run the test by the automated test system and determine whether it met the pass or fail criteria.

6. Reconfigure the test equipment or interfering signal level and repeat the test until the fail criteria is met. This indicates the susecptibility level has been reached.
7. Repeat the test on different test lines, or on more than one test line as needed.

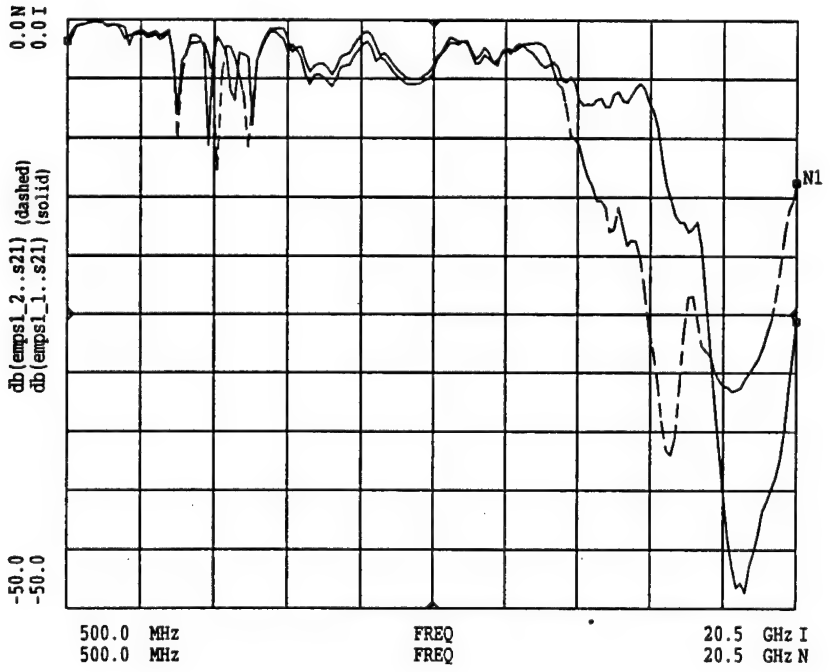


Figure 1: RF Characteristics of Diplexer 1-1

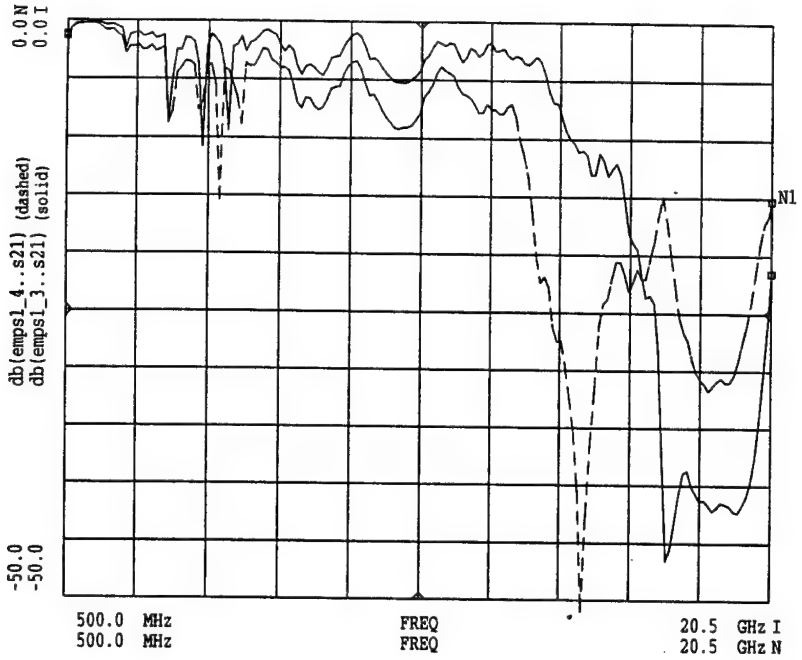


Figure 2: RF Characteristics of Diplexer 1-4

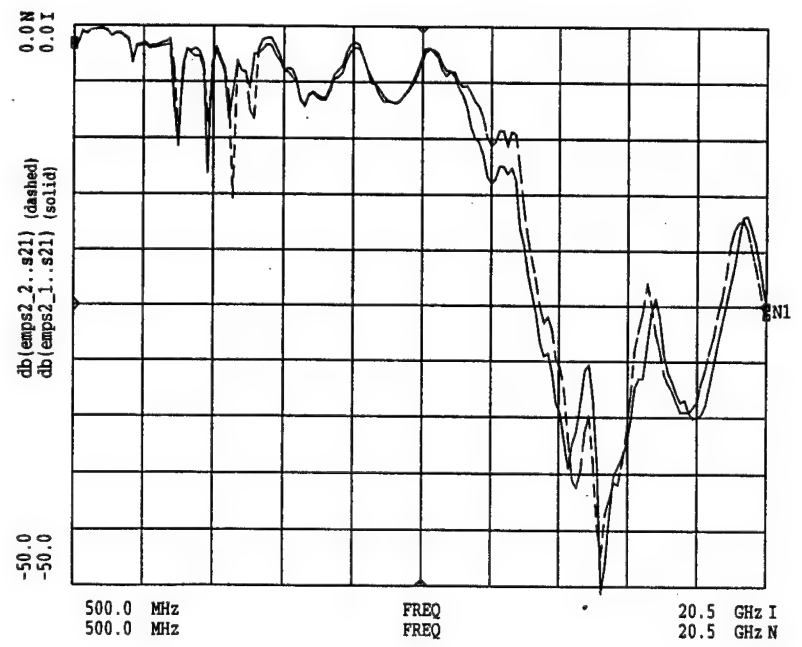


Figure 3: RF Characteristics of Diplexer 2-2

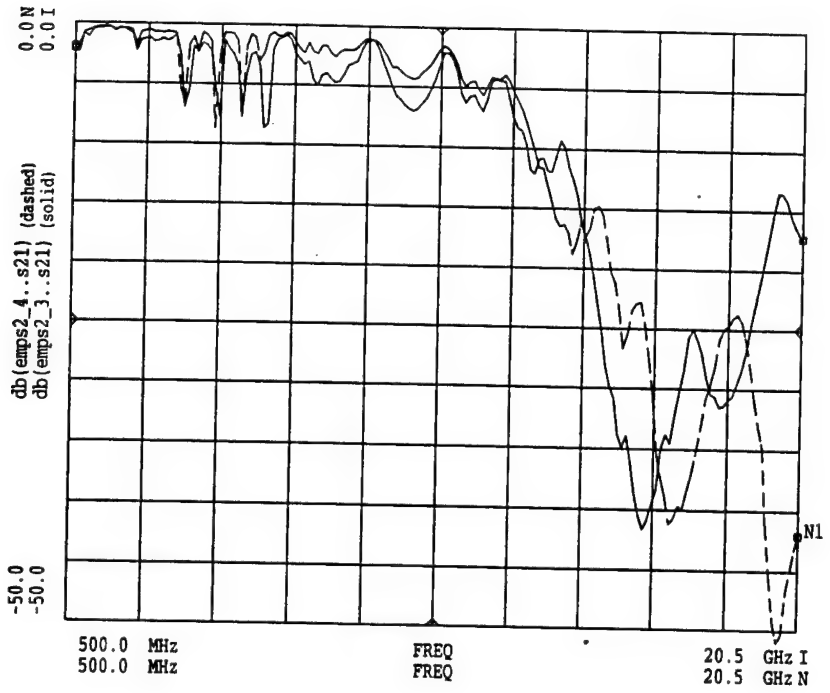


Figure 4: RF Characteristics of Diplexer 2-3

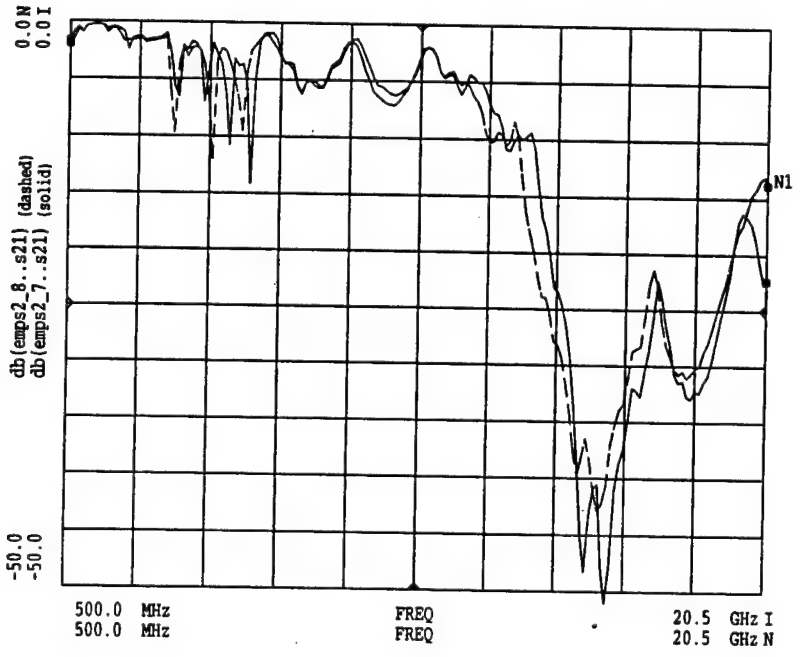


Figure 5: RF Characteristics of Diplexer 2-7

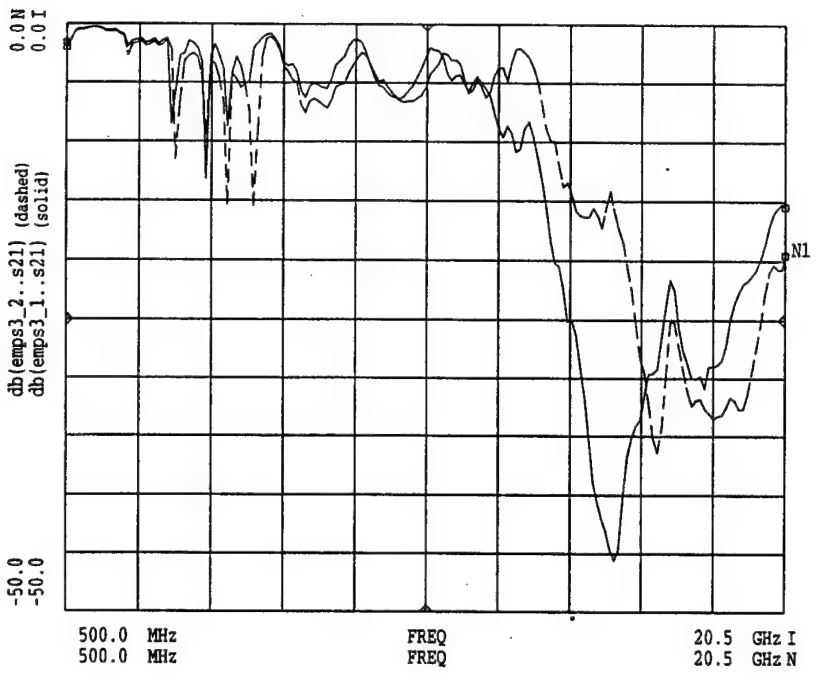


Figure 6: RF Characteristics of Diplexer 3-2

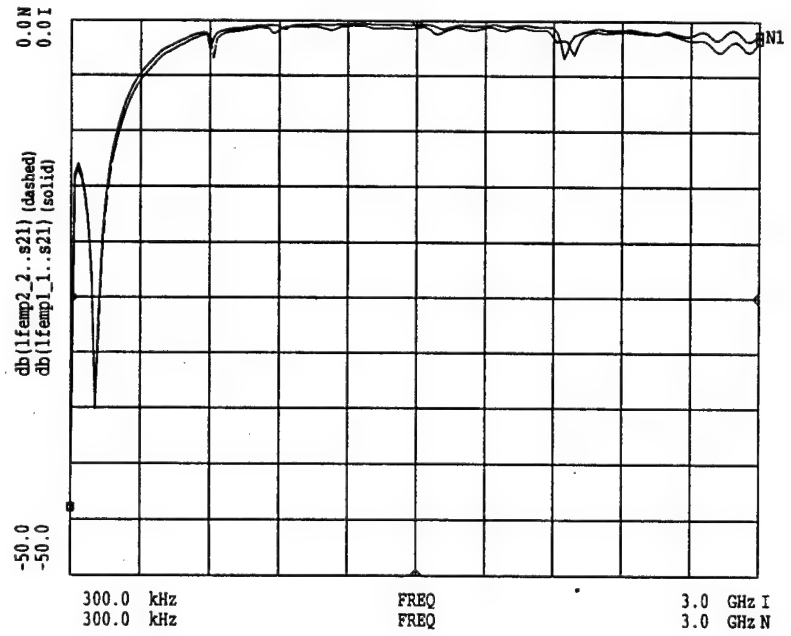


Figure 7: Low Frequency RF Characteristics of Diplexer 1-1

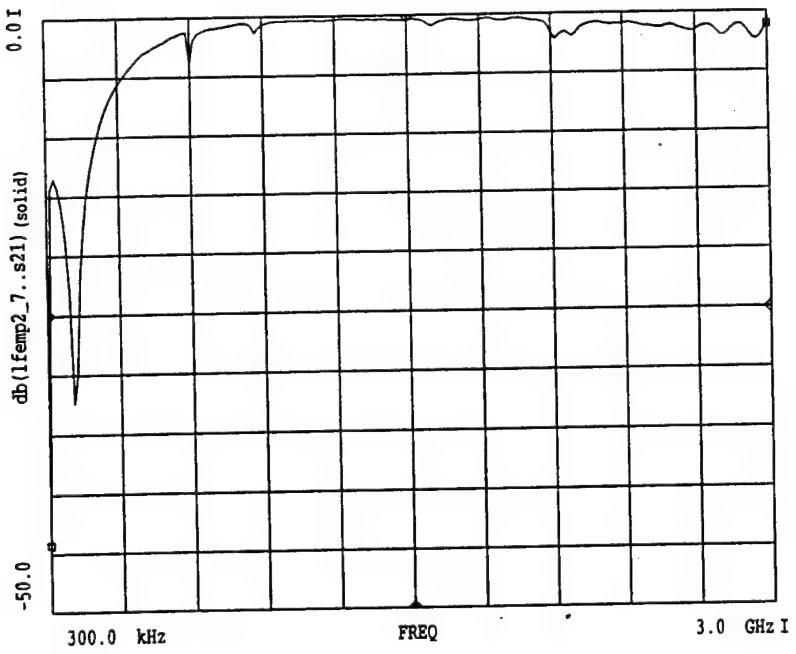


Figure 8: Low Frequency RF Characteristics of Diplexer 2-7

Frequency					RF				+15V Current
Range, GHz		Mfg.	Model	Gain	Pwr.	Case Size, Inches			Required
0.5	2	DBS	DBP-0102N533	40	2	0.67	1.56	2.91	1.4
2	6	DBS	DBP-0206N533	30	2	0.67	1.56	2.91	2
2	8	Cernex	CPA02083030	30	1	0.38	0.93	3.25	1.05
6	18	DBS	DPT-18616	32	1	0.67	1.56	3.66	2.5

Figure 9: Summary of Wide-band Amplifiers

W/B Amp P/N	S/N	Diplexer	Frequency	Gain
DBP18616	1	1-2	6	35
			9	32.5
			12	30.4
			15	15.5
			16	12.3
DBP18616	2	1-3	6	33.5
			9	29.5
			12	30
			15	20
			17	4
DBP0206N533	12	2-1	2	34.4
			4	30.6
			6	26.8
DBP0206N533	13	3-1	2	35.7
			4	32.8
			6	32.8
CPA02063230	2346	2-9	2	42.7
			4	42.8
			6	40.7
CPA02063230	2347	1-5	2	41.4
			4	38.5
			6	38.9
CPA02063230	2348	2-8	2	39.1
			4	37.9
			6	38.7
DBP0102N533	7	2-5	0.5	41.6
			1	43.7
			1.5	40.5
			2	40.3
DBP0102N533	8	2-6	0.5	41.8
			1	44.8
			1.5	42.1
			2	42.6
DBP0102N533	9	1-6	0.5	39.6
			1	40.9
			1.5	34.5
			2	35.9
DBP0102N533	10	2-4	0.5	40.9
			1	40
			1.5	35.5
			2	35.4

Figure 10: Gain Through Combined Diplexer/Wide-Band Amplifier

3DMM PIN #	SIGNAL NAME	3DMM Rt TF Pin	3DMM Left TF Pin	3DMM PIN #	SIGNAL NAME	3DMM Rt TF Pin	3DMM Left TF Pin
1	CAS5B	1		26	RAS4A		21
2	CAS6B	2		27	RAS3A		22
3	CAS7B	3		28	RAS2A		23
4	CAS8B	4		29	RAS1A		24
5	A1	5		30	DQ1		25
6	A3	6	1	31	DQ3	21	26
7	N/C	7	2	32	A8	22	27
8	A5	8	3	33	WE	23	28
9	RAS8B	9	4	34	CAS1A	24	29
10	RAS7B	10	5	35	CAS2A	25	30
11	RAS6B	11	6	36	CAS3A	26	31
12	RAS5B	12	7	37	CAS4A	27	32
13	VSS	13	8	38	VCC	28	33
14	CAS5A	14	9	39	RAS4B	29	34
15	CAS6A	15	10	40	RAS3B	30	35
16	CAS7A	16	11	41	RAS2B	31	36
17	CAS8A	17	12	42	RAS1B	32	37
18	A7	18	13	43	A6	33	38
19	G	19	14	44	A4	34	39
20	DQ4	20	15	45	A0	35	40
21	DQ2		16	46	A2	36	
22	RAS8A		17	47	CAS1B	37	
23	RAS7A		18	48	CAS2B	38	
24	RAS6A		19	49	CAS3B	39	
25	RAS5A		20	50	CAS4B	40	

Figure 11: Pin-out of 3DMM and Orientation in Test Fixture

PMM PIN #	TESTER CHANNEL	SIGNAL NAME	Adapt # 1	Bypass # 1	Adapt # 2	Bypass # 2	Adapt # 3	Bypass # 3
1								
2								
3								
4								
5								
6								
7								
8								
9								
10								
11								
12								
13	34	PMMFL	1			20		39
14	98	LWRITE	2			1		2
15	35	LADA	3			19		38
16	99	LAD31	4			2		3
17	36	LAD24	5			18		37
18	100	LAD5	6			3		4
19	37	LAD3	7			17		36
20	101	LAD1	8			4		5
21	38	LBA3	9			16		35
22	102	LBA1	10			5		6
23	39	INT3IN	11			15		34
24	103	INT2	12			6		7
25	40	INT0	13			14		33
26	104	FAIL0	14			7		8
27	41	MPER23	15			13		32
28	105	MPER21	16			8		9
29	42	MPER19	17			12		31
30	106	MPER17	18			9		10
31	43	MPER15	19			11		30
32	107		20		1			11
33	44	MPER13		1	2			29
34	108	MPER11		40	3			12
35	45	MPER9		2	4			28

Figure 12A: Pin-out of PMM and Orientation in Test Fixture

PMM PIN #	TESTER CHANNEL	SIGNAL NAME	Adapt # 1	Bypass # 1	Adapt # 2	Bypass # 2	Adapt # 3	Bypass # 3
36	109	MPER7		39	5			13
37	46	MPER5		3	6			27
38	110	MPER3		38	7			14
39	47	MPER1		4	8			26
40	111	MD31		37	9			15
41	48	MD29		5	10			25
42	112	MD27		36	11			16
43	49	MD25		6	12			24
44	113	MD23		35	13			17
45	50	MD21		7	14			23
46	114	MD19		34	15			18
47	51	MD17		8	16			22
48	115	MD15		33	17			19
49	52	MD13		9	18			21
50	116	MD11		32	19			20
51	53	MD9		10	20		1	
52	117	MA0		31		20	2	
53	54	MA2		11		2	3	
54	118	MA4		30		19	4	
55	55	MA6		12		3	5	
56	119	MA8		29		18	6	
57	56	MA10		13		4	7	
58	120	MA12		28		17	8	
59	57	MA14		14		5	9	
60	121	MA16		27		16	10	
61	58	MD1		15		6	11	
62	122	MD3		26		15	12	
63	59	MD5		16		7	13	
64	123	MD7		25		14	14	
65	60	WEIN		17		8	15	
66	124	CSE		24		13	16	
67				18		9	17	
68				23		12	18	
69	GND			19		10	19	
70	GND			22		11	20	

Figure 12B: Pin-out of PMM and Orientation in Test Fixture

PMM PIN #	TESTER CHANNEL	SIGNAL NAME	Adapt # 1	Bypass # 1	Adapt # 2	Bypass # 2	Adapt # 3	Bypass # 3
140								
139								
138								
137								
136								
135								
134								
133								
132								
131								
130								
129								
128			40			1		2
127			39			20		39
126			38			2		3
125			37			19		38
124			36			3		4
123			35			18		37
122			34			4		5
121			33			17		36
120			32			5		6
119			31			16		35
118			30			6		7
117			29			15		34
116			28			7		8
115			27			14		33
114			26			8		9
113	25	MPER22	25			13		32
112	88	MPER20	24			9		10
111	24	MPER18	23			12		31
110	87	MPER16	22			10		11
109			21		40			30
108	23	MPER14		40	39			12
107	86	MPER12		1	38			29
106	22	MPER10		39	37			13
105	85	MPER8		2	36			28

Figure 12C: Pin-out of PMM and Orientation in Test Fixture

PMM PIN #	TESTER CHANNEL	SIGNAL NAME	Adapt # 1	Bypass # 1	Adapt # 2	Bypass # 2	Adapt # 3	Bypass # 3
104	21	MPER6		38	35			14
103	84	MPER4		3	34			27
102	20	MPER2		37	33			15
101	83	MPER0		4	32			26
100	19	MD30		36	31			16
99	82	MD28		5	30			25
98	18	MD26		35	29			17
97	81	MD24		6	28			24
96	17	MD22		34	27			18
95	80	MD20		7	26			23
94	16	MD18		33	25			19
93	79	MD16		8	24			22
92	15	MD14		32	23			20
91	78	MD12		9	22			21
90	14	MD10		31	21		40	
89	77	MD8		10		1	39	
88	13	MA1		30		19	38	
87	76	MA3		11		2	37	
86	12	MA5		29		18	36	
85	75	MA7		12		3	35	
84	11	MA9		28		17	34	
83	74	MA11		13		4	33	
82	10	MA13		27		16	32	
81	73	MA15		14		5	31	
80	9	MD0		26		15	30	
79	72	MD2		15		6	29	
78	8	MD4		25		14	28	
77	71	MD6		16		7	27	
76	7	CSS2		24		13	26	
75	70	OE		17		8	25	
74	6	CSS		23		12	24	
73				18		9	23	
72	GND			22		11	22	
71	GND			19		10	21	

Figure 12D: Pin-out of PMM and Orientation in Test Fixture7

```
PRO MAIN PINS
WRITE *

;*************************************************************************
;*                                                                       *
;*      EVALUATION TEST PROGRAM FOR TEXAS INSTRUMENTS 4M X 4             *
;*      DRAM STACKED MEMORY MODULE                                       *
;*                                                                       *
;*************************************************************************

;---------GLOBAL VARIABLES-------------

;DATASET NUMBER
STRING DATASET(35)=""

;PART NUMBER
STRING PRTNMBR(25)="SMM"

;PROGRAMMER/AUTHOR
STRING PRGMER(15)="J.L.SHAVER"

;RELEASE DATE
STRING RELDATE(15)="08-SEP-1998"

;REQUIREMENTS
STRING REQS(35)=""

;LOAD BOARD
STRING LDBRD(15)="0009"

;LOAD BOARD ID NUMBER - SET WITH ROTARY SWITCHES ON THE PERFORMANCE BOARD
INTEGER BRDID=#0009

;*************************************************************************
;
;               PIN CONNECTION LIST
;
;*************************************************************************
;
;       TESTER  PIN          DEVICE      PIN     TESTER
;       CHANNEL NAME          PIN        NAME    CHANNEL
;       ------- ----      -----------    ----    -------
;
;                         +----V----+
;          133  CAS5B     I  1   50 I   CAS4B   185
;          134  CAS6B     I  2   49 I   CAS3B   186
;          135  CAS7B     I  3   48 I   CAS2B   187
;          136  CAS8B     I  4   47 I   CAS1B   188
;     (74)  73  A1        I  5   46 I   A2      181 (182)
;     (76)  75  A3        I  6   45 I   A0      183 (184)
;          137  N/C       I  7   44 I   A4      53  (54)
;    (140) 139  A5        I  8   43 I   A6      55  (56)
;          141  RAS8B     I  9   42 I   RAS1B   177
;          142  RAS7B     I 10   41 I   RAS2B   178
;          143  RAS6B     I 11   40 I   RAS3B   179
;          144  RAS5B     I 12   39 I   RAS4B   180
;          GND  VSS       I 13   38 I   VCC     PS1
;          145  CAS5A     I 14   37 I   CAS4A   173
;          146  CAS6A     I 15   36 I   CAS3A   174
;          147  CAS7A     I 16   35 I   CAS2A   175
```

```
;          148  CAS8A      I 17   34 I   CAS1A   176
;     (22)  21  A7         I 18   33 I   WE      45
;           23  G          I 19   32 I   A8      47  (48)
;          149  DQ4        I 20   31 I   DQ3     41
;          150  DQ2        I 21   30 I   DQ1     42
;           28  RAS8A      I 22   29 I   RAS1A   165
;           27  RAS7A      I 23   28 I   RAS2A   166
;           26  RAS6A      I 24   27 I   RAS3A   167
;           25  RAS5A      I 25   26 I   RAS4A   168
;                          +---------+
;
;
;*************************************************************************

;*************************************
;*             PINLISTS              *
;*************************************

PINLIST ROWADD = P32,18,43,8,44,6,46,5,45        ;X8->X0

PINLIST COLADD = P59-51          ;Y8->Y0

PINLIST RASA = P22-29            ;RAS8A->RAS1A
PINLIST RASB = P9-12,39-42       ;RAS8B->RAS1B
PINLIST RAS  = RASA,RASB

PINLIST CASA = P17-14,37-34      ;CAS8A->CAS1A
PINLIST CASB = P4-1,50-47        ;CAS8B->CAS1B
PINLIST CAS  = CASA,CASB

PINLIST DQ = P20,31,21,30        ;DQ4->DQ1

PINLIST ALLIN = P1-6,8,10-12,14-37,39-50         ;NOTE P9 REMOVED

;*************************************
;*            VARIABLES              *
;*************************************

INTEGER TNUM=1
INTEGER SERIAL                   ;SERIAL NUMBER OF PART BEING TESTED
INTEGER FCNT                     ;COUNTER TO HOLD NUMBER OF TESTS THAT FAILED
INTEGER LIMCOND                  ;FLAG FOR JUDGING MIN AND/OR MAX LIMITS
INTEGER SERNUM                   ;SERIAL NUMBER OF DUT - FOR OUTPUT ROUTINE
INTEGER MINTYP                   ;FLAG USED IN OUTPUT ROUTINE
INTEGER MAXTYP                   ;FLAG USED IN OUTPUT ROUTINE
INTEGER RCODE                    ;FLAG USED IN OUTPUT ROUTINE
INTEGER SEL                      ;HOLDS MENU SELECTION
INTEGER PN                       ;COUNT CONTACT FAIL PINS
INTEGER BADBOY                   ;FAILED PIN NUMBER
GENERAL BADDAT                   ;FAIL DATA
REAL MAXLIM                      ;MAXIMUM LIMIT FOR EACH TEST(0 - NO LIMIT)
REAL MINLIM                      ;MINIMUM LIMIT FOR EACH TEST(0 - NO LIMIT)
STRING PF(8)                     ;PASS OR FAIL FOR OUTPUT
STRING TSYM(8)                   ;TEST SYMBOL FOR OUTPUT
STRING TCOND(8)

DIM XPIN(50)                     ;HOLD CONTACT FAIL PINS
DIM IPINS(43)="CAS5B","CAS6B","CAS7B","CAS8B","A1","A3","A5","RAS8B","RAS7B",@
"RAS6B","RAS5B","CAS5A","CAS6A","CAS7A","CAS8A","A7","G","RAS8A","RAS7A",@
"RAS6A","RAS5A","RAS4A","RAS3A","RAS2A","RAS1A","A8","WE","CAS1A","CAS2A",@
```

```
"CAS3A","CAS4A","RAS4B","RAS3B","RAS2B","RAS1B","A6","A4","A0","A2","CAS1B",@
"CAS2B","CAS3B","CAS4B"

DIM OPINS(4)="DQ4","DQ3","DQ2","DQ1"

INTEGER NOINS=43
INTEGER NOOUTS=4

DEFINE REAL RES(200)

;*****************************************************************************


;#############################################################################
;
;       MAIN PROGRAM
;
;#############################################################################

FCNT = 0        ;INITIALIZE THE FAIL COUNT

;IF INIT KEY HAS BEEN PUNCHED, DISPLAY PROGRAM INFORMATION
IF INIT THEN GOSUB DOINIT

GOSUB DOHEAD
GOSUB DOTESTS
GOSUB DOFOOT
STOP
;#############################################################################
;
;       MAIN TEST ROUTINE
;
;#############################################################################
DOTESTS:
;************************************
;*     TEST FOR PERFORMANCE BOARD    *
;************************************
SET DISPLAY "CONTACT.."
    VS1=0V
    ISVM MDC=-10UA,M(8V),2V,-2V
    LIMIT MDC = 1.5V,-1.5V
    MEAS MDC(ALLIN)
    IF FAIL THEN ENTRY
        WRITE $4 "**CONTACT FAILURE**"  ,//
        READ FPIN TO PN,XPIN
        WRITE [1,1],"NUMBER OF CONTACT FAILS: ",PN,//
        WRITE "PINS:",//
        DO CNTCT I=1,PN
                BADBOY = XPIN(I)
                READ DCT PDATA(P(BADBOY)) TO BADDAT
                WRITE BADBOY
                WRITE [1,2],BADDAT,/
        CNTCT:
        STOP
    EXIT
SET DISPLAY "         "

;************************************
;*      GROSS FUNCTIONAL TEST        *
;************************************
```

```
SET DISPLAY "GRFUNC"
TSYM     = "GRFUNC"
TCOND    = "500KHZ"
MAXLIM   = 0
MINLIM   = 0
GOSUB PIN1
GOSUB REF1
GOSUB VIN1
GOSUB TIM1
SELECT PDS ALPG
SELECT LPAT NORMAL

TEST TNUM

CALL CALB("FUNC","NORMAL")
GOTO SKIP1
REG LPAT STA=#50
MEAS LPAT FUNC
IF FAIL THEN RES(TNUM)=0HZ
ELSE RES(TNUM)=1HZ
GOSUB OUTPUT
SKIP1:
TNUM=TNUM+1

SET DISPLAY "MATS++"
TSYM     = "MATS++"
TEST TNUM
REG LPAT STA=#50
REG LPAT SPA=#124
MEAS LPAT MATS
IF FAIL THEN RES(TNUM)=0HZ
ELSE RES(TNUM)=1HZ
GOSUB OUTPUT
TNUM=TNUM+1

;*********************************
;*       DYNAMIC TEST MENU       *
;*********************************

SET DISPLAY "TEST MENU"
TEST TNUM

MENUB:
GOSUB MENU
GOSUB GETSEL
GOTO (SEL) D1A,D2A,D3A,D4A,D5A,D6A,D7A,D8A,@
           D1B,D2B,D3B,D4B,D5B,D6B,D7B,MENUE,MENUB
D1A:    WRITE [1],/,"TESTING DRAM 1A",/
        TSYM="DRAM1A"
        REG LPAT STA=#150
        REG LPAT SPA=#160
        MEAS LPAT MATS
        IF FAIL THEN RES(TNUM)=0HZ
        ELSE RES(TNUM)=1HZ
        GOSUB OUTPUT
        GOTO MENUB
D2A:    WRITE [1],/,"TESTING DRAM 2A",/
        TSYM="DRAM2A"
        REG LPAT STA=#160
        REG LPAT SPA=#170
```

```
        MEAS LPAT MATS
        IF FAIL THEN RES(TNUM)=0HZ
        ELSE RES(TNUM)=1HZ
        GOSUB OUTPUT
        GOTO MENUB
D3A:    WRITE [1],/,"TESTING DRAM 3A",/
        TSYM="DRAM3A"
        REG LPAT STA=#170
        REG LPAT SPA=#180
        MEAS LPAT MATS
        IF FAIL THEN RES(TNUM)=0HZ
        ELSE RES(TNUM)=1HZ
        GOSUB OUTPUT
        GOTO MENUB
D4A:    WRITE [1],/,"TESTING DRAM 4A",/
        TSYM="DRAM4A"
        REG LPAT STA=#180
        REG LPAT SPA=#190
        MEAS LPAT MATS
        IF FAIL THEN RES(TNUM)=0HZ
        ELSE RES(TNUM)=1HZ
        GOSUB OUTPUT
        GOTO MENUB
D5A:    WRITE [1],/,"TESTING DRAM 5A",/
        TSYM="DRAM5A"
        REG LPAT STA=#1A0
        REG LPAT SPA=#1B0
        MEAS LPAT MATS
        IF FAIL THEN RES(TNUM)=0HZ
        ELSE RES(TNUM)=1HZ
        GOSUB OUTPUT
        GOTO MENUB
D6A:    WRITE [1],/,"TESTING DRAM 6A",/
        TSYM="DRAM6A"
        REG LPAT STA=#1B0
        REG LPAT SPA=#1C0
        MEAS LPAT MATS
        IF FAIL THEN RES(TNUM)=0HZ
        ELSE RES(TNUM)=1HZ
        GOSUB OUTPUT
        GOTO MENUB
D7A:    WRITE [1],/,"TESTING DRAM 7A",/
        TSYM="DRAM7A"
        REG LPAT STA=#1C0
        REG LPAT SPA=#1D0
        MEAS LPAT MATS
        IF FAIL THEN RES(TNUM)=0HZ
        ELSE RES(TNUM)=1HZ
        GOSUB OUTPUT
        GOTO MENUB
D8A:    WRITE [1],/,"TESTING DRAM 8A",/
        TSYM="DRAM1A"
        REG LPAT STA=#1D0
        REG LPAT SPA=#1E0
        MEAS LPAT MATS
        IF FAIL THEN RES(TNUM)=0HZ
        ELSE RES(TNUM)=1HZ
        GOSUB OUTPUT
        GOTO MENUB
D1B:    WRITE [1],/,"TESTING DRAM 1B",/
```

```
        TSYM="DRAM1B"
        REG LPAT STA=#1E0
        REG LPAT SPA=#1F0
        MEAS LPAT MATS
        IF FAIL THEN RES(TNUM)=0HZ
        ELSE RES(TNUM)=1HZ
        GOSUB OUTPUT
        GOTO MENUB
D2B:    WRITE [1],/,"TESTING DRAM 2B",/
        TSYM="DRAM2B"
        REG LPAT STA=#1F0
        REG LPAT SPA=#200
        MEAS LPAT MATS
        IF FAIL THEN RES(TNUM)=0HZ
        ELSE RES(TNUM)=1HZ
        GOSUB OUTPUT
        GOTO MENUB
D3B:    WRITE [1],/,"TESTING DRAM 3B",/
        TSYM="DRAM3B"
        REG LPAT STA=#200
        REG LPAT SPA=#210
        MEAS LPAT MATS
        IF FAIL THEN RES(TNUM)=0HZ
        ELSE RES(TNUM)=1HZ
        GOSUB OUTPUT
        GOTO MENUB
D4B:    WRITE [1],/,"TESTING DRAM 4B",/
        TSYM="DRAM4B"
        REG LPAT STA=#210
        REG LPAT SPA=#220
        MEAS LPAT MATS
        IF FAIL THEN RES(TNUM)=0HZ
        ELSE RES(TNUM)=1HZ
        GOSUB OUTPUT
        GOTO MENUB
D5B:    WRITE [1],/,"TESTING DRAM 5B",/
        TSYM="DRAM5B"
        REG LPAT STA=#220
        REG LPAT SPA=#230
        MEAS LPAT MATS
        IF FAIL THEN RES(TNUM)=0HZ
        ELSE RES(TNUM)=1HZ
        GOSUB OUTPUT
        GOTO MENUB
D6B:    WRITE [1],/,"TESTING DRAM 6B",/
        TSYM="DRAM6B"
        REG LPAT STA=#230
        REG LPAT SPA=#240
        MEAS LPAT MATS
        IF FAIL THEN RES(TNUM)=0HZ
        ELSE RES(TNUM)=1HZ
        GOSUB OUTPUT
        GOTO MENUB
D7B:    WRITE [1],/,"TESTING DRAM 7B",/
        TSYM="DRAM7B"
        REG LPAT STA=#240
        REG LPAT SPA=#250
        MEAS LPAT MATS
        IF FAIL THEN RES(TNUM)=0HZ
        ELSE RES(TNUM)=1HZ
```

```
        GOSUB OUTPUT
        GOTO MENUB

MENUE:

;*************************************
;*      DYNAMIC SUPPLY CURRENT       *
;*************************************
SET DISPLAY "ICC"
TSYM    = "ICC"
TCOND   = "11.1MHZ"
MAXLIM  = 160MA
MINLIM  = 0

GOSUB PIN1
GOSUB REF1
GOSUB VIN1
GOSUB TIM1

VSIM UDC = 5.5V,R8V,M(300MA),1A,-1A
TEST TNUM

MCON=1
CALL CALB("ICC","NORMAL")
SEND LPAT FUNC
REG LPAT STA=#50
SRON
START LPAT *
MEAS UDC:RES(TNUM)
STOP LPAT
SROF

MCON=0

GOSUB OUTPUT
TNUM=TNUM+1

GOTO CONTINUE

;*************************************
;*     OUTPUT LEAKAGE CURRENT LOW    *
;*************************************
SET DISPLAY "IOZL"
TSYM    = "IOZL"
MAXLIM  = 10UA
MINLIM  = -10UA

GOSUB PIN1
GOSUB REF1
GOSUB VIN1
GOSUB TIM1

VSIM UDC=0.0V,M(AUTO)

DO IOLL I=1,NOOUTS

   DQ(I)=UDC
   TEST TNUM
   MEAS UDC:RES(TNUM)
   SROF
```

```
   TCOND = OPINS(I)
   GOSUB OUTPUT
   TNUM=TNUM+1

IOLL:

;*************************************
;*     OUTPUT LEAKAGE CURRENT HIGH    *
;*************************************
SET DISPLAY "IOZH"
TSYM    = "IOZH"
MAXLIM  = 10UA
MINLIM  = -10UA

GOSUB PIN1
GOSUB REF1
GOSUB VIN1
GOSUB TIM1

VSIM UDC=5.5V,M(AUTO)

DO IOLH I=1,NOOUTS

   DQ(I)=UDC
   TEST TNUM
   MEAS UDC:RES(TNUM)
   SROF
   TCOND = OPINS(I)
   GOSUB OUTPUT
   TNUM=TNUM+1

IOLH:

;*************************************
;*    INPUT LEAKAGE CURRENT - LOW     *
;*************************************
SET DISPLAY "IIL"
TSYM    = "IIL"
MAXLIM  = 10UA
MINLIM  = -10UA

GOSUB PIN1
GOSUB REF1
GOSUB VIN1
GOSUB TIM1

VSIM UDC=0.0V,M(AUTO)

DO ILIL I=1,NOINS

   ALLIN(I)=UDC
   TEST TNUM
   MEAS UDC:RES(TNUM)
   SROF
   TCOND = IPINS(I)
   GOSUB OUTPUT
   TNUM=TNUM+1
ILIL:

;*************************************
```

```
;*     INPUT LEAKAGE CURRENT - HIGH    *
;************************************
SET DISPLAY "IIH"
TSYM     = "IIH"
MAXLIM   = 10UA
MINLIM   = -10UA

DO ILIH I=1,NOINS
  SELECT RETRY ENABLE
  VSIM UDC=5.5V,M(AUTO)
  ALLIN(I)=UDC
  TEST TNUM
  MEAS UDC:RES(TNUM)
  SROF
  TCOND = IPINS(I)
  GOSUB OUTPUT
  TNUM=TNUM+1
ILIH:
SELECT RETRY DISABLE

;*********************************
;*      OUTPUT VOLTAGE - LOW      *
;*********************************
SET DISPLAY "VOL"
TSYM     = "VOL"
MAXLIM   = 0.4V
MINLIM   = 0

GOSUB PIN1
GOSUB REF1
GOSUB VIN1
GOSUB TIM1

CALL CALB("GFUNC","NORMAL")

DO VOLA I=1,NOOUTS

   DQ(I)=IN3,NRZA,ACLK2,OUT2,STRB1,IL1,VT1,DRE1,DRERZ,<FIXL>
   HI=1.5V
   LO=0.01V
   TRY=0.7V

   VOL1:
        OUT2=2.4V,TRY

        TEST TNUM
        MEAS LPAT GRFUNC
        IF FAIL THEN LO=TRY
           ELSE HI=TRY
        TRY=(HI-LO)/2+LO
        IF HI-TRY>2.0MV THEN GOTO VOL1

        RES(TNUM)=TRY
        TCOND = OPINS(I)
        GOSUB OUTPUT
        DQ(I)=IN3,NRZA,ACLK2,OUT1,STRB1,IL1,VT1,DRE1,DRERZ,<FIXL>
        TNUM=TNUM+1
VOLA:

;************************************
```

```
;*      OUTPUT VOLTAGE - HIGH          *
;*************************************
SET DISPLAY "VOH"
TSYM      = "VOH"
MAXLIM    = 0
MINLIM    = 2.4V

CALL CALB("GFUNC","NORMAL")
DO VOHA I=1,NOOUTS

   DQ(I)=IN3,NRZA,ACLK2,OUT2,STRB1,IL1,VT1,DRE1,DRERZ,<FIXH>
   HI=5.0V
   LO=1.0V
   TRY=2.4V

   VOH1:
        OUT2=TRY,0.8V
        TEST TNUM
        MEAS LPAT GRFUNC
        IF FAIL THEN HI=TRY
        ELSE LO=TRY
        TRY=(HI-LO)/2+LO
        IF HI-TRY>2.0MV THEN GOTO VOH1

        RES(TNUM)=TRY
        TCOND = OPINS(I)
        GOSUB OUTPUT
        DQ(I)=IN3,NRZA,ACLK2,OUT1,STRB1,IL1,VT1,DRE1,DRERZ,<FIXH>
        TNUM=TNUM+1
VOHA:

;*************************************************
;*        INPUT VOLTAGE - LOW (ADBUS_L)          *
;*************************************************
SET DISPLAY "VIL"
TSYM = "VIL"
TCOND = "ADBUS_L"
MINLIM = 0.8V
MAXLIM = 0
HI=3.0V
LO=0.01V
TRY=50MV

TEST TNUM
ROWADD=IN2,NRZA,ACLK1,<X8-0>

VIL1:
        TEST TNUM
        IN2=3V,TRY
        MEAS LPAT FUNC
        IF FAIL THEN HI=TRY
                ELSE LO=TRY
        TRY=(HI-LO)/2+LO
        IF HI-TRY>2.0MV THEN GOTO VIL1

RES(TNUM)=TRY
GOSUB OUTPUT
TNUM=TNUM+1

;*************************************************
```

```
;*       INPUT VOLTAGE - LOW (DATA BUSES)        *
;************************************************

;DBUSL=IN2,NRZA,ACLK2,OUT1,STRB1,IL1,VT1,DRE1,DRERZ,<D0-7>
;DBUSR=IN2,NRZA,ACLK2,OUT1,STRB1,IL1,VT1,DRE1,DRERZ,<D10-17>

HI=3.0V
LO=0.01V
TRY=50MV
TEST TNUM

VIL3:

        IN2=3V,TRY
        MEAS LPAT FUNC
        IF FAIL THEN HI=TRY
                ELSE LO=TRY
        TRY=(HI-LO)/2+LO
        IF HI-TRY>2.0MV THEN GOTO VIL3

RES(TNUM)=TRY
TCOND(1,8)="DATA BUS"
GOSUB OUTPUT
TNUM=TNUM+1
;DBUSL=IN3,NRZA,ACLK2,OUT1,STRB1,IL1,VT1,DRE1,DRERZ,<D0-7>
;DBUSR=IN3,NRZA,ACLK2,OUT1,STRB1,IL1,VT1,DRE1,DRERZ,<D10-17>

;************************************************
;*       INPUT VOLTAGE - LOW (/WE PINS)         *
;************************************************

HI=3.0V
LO=0.01V
TRY=20MV
TEST TNUM
;WEPINS   =  IN2,/RZZ,BCLK1

VIL4:

        IN2=3V,TRY
        MEAS LPAT GRFUNC
        IF FAIL THEN HI=TRY
                ELSE LO=TRY
        TRY=(HI-LO)/2+LO
        IF HI-TRY>2.0MV THEN GOTO VIL4

RES(TNUM)=TRY
;WEPINS   =  IN1,/RZZ,BCLK1
TCOND(1,8)=" WE PINS"
GOSUB OUTPUT
TNUM=TNUM+1

;************************************************
;*       INPUT VOLTAGE - LOW (/CE PINS)         *
;************************************************

;CEL   =  IN2,/RZZ,BCLK2
;CER   =  IN2,/RZZ,BCLK3
HI=3.0V
LO=0.01V
```

```
TRY=50MV
TEST TNUM

VIL5:

        IN2=3V,TRY

        MEAS LPAT GRFUNC
        IF FAIL THEN HI=TRY
                ELSE LO=TRY
        TRY=(HI-LO)/2+LO
        IF HI-TRY>2.0MV THEN GOTO VIL5

RES(TNUM)=TRY
;CEL    =  IN1,/RZZ,BCLK2
;CER    =  IN1,/RZZ,BCLK3
TCOND(1,8)=" CE PINS"
GOSUB OUTPUT
TNUM=TNUM+1

;*************************************************
;*       INPUT VOLTAGE - LOW (/OE PINS)          *
;*************************************************

;OEPINS    =  IN2,/RZZ,BCLK4
HI=3.0V
LO=0.01V
TRY=50MV
TEST TNUM
VIL6:

        IN2= 3V,TRY

        MEAS LPAT GRFUNC
        IF FAIL THEN HI=TRY
                ELSE LO=TRY
        TRY=(HI-LO)/2+LO
        IF HI-TRY>2.0MV THEN GOTO VIL6

RES(TNUM)=TRY
;OEPINS    =  IN1,/RZZ,BCLK4
TCOND(1,8)=" OE PINS"
GOSUB OUTPUT
TNUM=TNUM+1

;*************************************
;*       INPUT VOLTAGE - HIGH        *
;*************************************
SET DISPLAY "VIH"
TSYM    = "VIH"
MAXLIM = 2.2V
MINLIM = 0

;*********VIH FOR ADDRESS BUS LEFT*********

;ADBUSL=IN2,NRZA,ACLK1,<X0-10>

HI=3.0V
LO=1.0V
TRY=3.0V
```

```
TEST TNUM

VIH1:

        IN2     =  TRY,0.0V
        MEAS LPAT GRFUNC
        IF FAIL THEN LO=TRY
                ELSE HI=TRY
        TRY=(HI-LO)/2+LO
        IF HI-TRY>2.0MV THEN GOTO VIH1

RES(TNUM)=TRY
;ADBUSL=IN1,NRZA,ACLK1,<X0-10>
TCOND(1,8)=" ADBUS_L"
GOSUB OUTPUT
TNUM=TNUM+1

;***********VIH FOR DATA BUS**********

;DBUSL=IN2,NRZA,ACLK2,OUT1,STRB1,IL1,VT1,DRE1,DRERZ,<D0-7>
;DBUSR=IN2,NRZA,ACLK2,OUT1,STRB1,IL1,VT1,DRE1,DRERZ,<D10-17>

HI=3.0V
LO=1.0V
TRY=3.0V
TEST TNUM

VIH3:

        IN2=TRY,0.0V
        MEAS LPAT GRFUNC
        IF FAIL THEN LO=TRY
                ELSE HI=TRY
        TRY=(HI-LO)/2+LO
        IF HI-TRY>2.0MV THEN GOTO VIH3

RES(TNUM)=TRY
;DBUSL=IN3,NRZA,ACLK2,OUT1,STRB1,IL1,VT1,DRE1,DRERZ,<D0-7>
;DBUSR=IN3,NRZA,ACLK2,OUT1,STRB1,IL1,VT1,DRE1,DRERZ,<D10-17>
TCOND(1,8)="DATA BUS"
GOSUB OUTPUT
TNUM=TNUM+1

;**********VIH ON /WE PINS*************

;WEPINS    =  IN2,/RZZ,BCLK1

HI=3.0V
LO=1.0V
TRY=3.0V
TEST TNUM

VIH4:

        IN2=TRY,0.0V
        MEAS LPAT GRFUNC
        IF FAIL THEN LO=TRY
                ELSE HI=TRY
        TRY=(HI-LO)/2+LO
        IF HI-TRY>2.0MV THEN GOTO VIH4
```

```
RES(TNUM)=TRY
;WEPINS    =  IN1,/RZZ,BCLK1
TCOND(1,8)=" WE PINS"
GOSUB OUTPUT
TNUM=TNUM+1

;**********VIH ON /CE PINS*************

;CEL    =  IN2,/RZZ,BCLK2
;CER    =  IN2,/RZZ,BCLK3
HI=3.0V
LO=1.0V
TRY=3.0V
TEST TNUM

VIH5:

        IN2=TRY,0.0V
        MEAS LPAT GRFUNC
        IF FAIL THEN LO=TRY
                ELSE HI=TRY
        TRY=(HI-LO)/2+LO
        IF HI-TRY>2.0MV THEN GOTO VIH5

RES(TNUM)=TRY
;CEL    =  IN1,/RZZ,BCLK2
;CER    =  IN1,/RZZ,BCLK3
TCOND(1,8)=" CE PINS"
GOSUB OUTPUT
TNUM=TNUM+1

;**********VIH ON /OE PINS*************

;OEPINS    =  IN2,/RZZ,BCLK4
HI=3.0V
LO=1.0V
TRY=3.0V
TEST TNUM

VIH6:

        IN2=TRY,0.0V
        MEAS LPAT GRFUNC
        IF FAIL THEN LO=TRY
                ELSE HI=TRY
        TRY=(HI-LO)/2+LO
        IF HI-TRY>2.0MV THEN GOTO VIH6

RES(TNUM)=TRY
;OEPINS    =  IN1,/RZZ,BCLK4
TCOND(1,8)=" OE PINS"
GOSUB OUTPUT
TNUM=TNUM+1

GOTO CONTINUE   ;********* END OF TESTS ***********

;************************************
;*     DATA OUTPUT SUBROUTINE       *
;************************************
```

```
OUTPUT:

TCOND=ASCII(TCOND,2,8)
TSYM=ASCII(TSYM,2,8)
LIMCOND=0                                   ;INITIALIZE FOR BOTH MAX & MIN LIMITS
PF="PASS     "                              ;ASSUME INNOCENT UNTIL PROVEN GUILTY
OMIN=MINLIM                                 ;INITIALIZE MIN LIMIT OUTPUT VARIABLE
OMAX=MAXLIM                                 ;INITIALIZE MAX LIMIT OUTPUT VARIABLE

MINTYP=CODE(MINLIM)
MAXTYP=CODE(MAXLIM)

IF MINTYP=2 AND MAXTYP<>2 THEN LIMCOND=1;NO MINIMUM LIMIT
IF MAXTYP=2 AND MINTYP<>2 THEN LIMCOND=2;NO MAXIMUM LIMIT
IF MAXTYP=2 AND MINTYP=2 THEN LIMCOND=3 ;NEITHER MAX LIMIT OR MIN LIMIT

IF LIMCOND=0 THEN ENTRY                     ;JUDGE BOTH LIMITS
        IF RES(TNUM)<MINLIM OR RES(TNUM)>MAXLIM THEN PF="FAIL ***"
        EXIT

IF LIMCOND=1 THEN ENTRY                     ;JUDGE ONLY MAXIMUM LIMIT
        OMIN="NONE      "
        IF RES(TNUM)>MAXLIM THEN PF="FAIL ***"
        EXIT

IF LIMCOND=2 THEN ENTRY                     ;JUDGE ONLY MINIMUM LIMIT
        OMAX="NONE      "
        IF RES(TNUM)<MINLIM THEN PF="FAIL ***"
        EXIT

IF LIMCOND=3 THEN ENTRY                     ;TEST IS FUNCTIONAL, NO JUDGE LIMITS
        OMAX="NONE      "
        OMIN="NONE      "
        IF RES(TNUM)=0HZ THEN PF="FAIL ***"
        EXIT

IF PF(1,1)="F" THEN ENTRY
        FCNT=FCNT+1                          ; TRACK TOTAL # OF FAILED TESTS
        EXIT

IF FK=.1 THEN ENTRY
        WRITE [1,2(6,0)] TNUM,"   "
        WRITE [1,4(8,0)] TSYM,"   "
        WRITE [1,4(8,0)] TCOND,"   "
        WRITE [1,2(11,3)] OMAX,"   "
        WRITE [1,2(11,3)] OMIN,"   "
        RCODE=CODE(RES(TNUM))
        IF RCODE=2 THEN WRITE [1,2(8,3)] RES(TNUM),"      "
                   ELSE WRITE [1,2(11,3)] RES(TNUM),"   "
        WRITE [1,2(9,3)] PF,/
EXIT

GOTO CONTINUE

;#############################################################################
;
;       WRITE FOOTER ROUTINE
;
;#############################################################################
DOFOOT:
```

```
READ CNT99 TO SERNUM
IF FCNT=0 THEN ENTRY
  WRITE [1] / "SERIAL NUMBER ",SERNUM,"PASSES" /
  RESET RESULT 3
EXIT
ELSE ENTRY
  WRITE [1] / "SERIAL NUMBER ",SERNUM,"** FAILS **" /
  SET RESULT 3
EXIT

GOTO CONTINUE
;#############################################################################
;
;       WRITE HEADER ROUTINE
;
;#############################################################################
DOHEAD:

STRING XTIME(17)

IF FK=.1 THEN ENTRY
  WRITE ?<14>?

  WRITE [1] "DATASET:      " DATASET /
  WRITE [1] "PART NUMBER:  " PRTNMBR /
  XTIME=GDAY(1)
  WRITE [1] "DATE:         " XTIME /
  READ CNT99 TO SERNUM
  WRITE [1] "SERIAL NO.:   " SERNUM //

  WRITE [1] " TEST      SYM       COND      MAXIMUM      MINIMUM      RESULT
  WRITE [1] "------  ---------  -------  -----------  -----------  -----------
EXIT

GOTO CONTINUE

;#############################################################################
;
;       INITIALIZATION ROUTINE
;
;#############################################################################
DOINIT:

RESET DISPLAY
WRITE [1] ?<14>?

WRITE [1] // "DATASET:        " DATASET /
WRITE [1]    "PART NUMBER:    " PRTNMBR /
WRITE [1]    "AUTHOR:         " PRGMER /
WRITE [1]    "RELEASE DATE:   " RELDATE /
WRITE [1]    "REQUIREMENTS:   " REQS /
WRITE [1,5(4)]    "LOAD BOARD:    " BRDID //

WRITE [1] "NOTE: DATA LOGGING IS CONTROLLED BY FUNCTION KEY #1.  DATA LOG" /
WRITE [1] "      DESTINATION IS SET USING THE 'S' CONTROLLER COMMAND." //

INIT1:
WRITE [1]      "PRESS <S> TO STOP",/
INPUT [1,4(0)] "       <C> TO CONTINUE ",C,/
```

```
IF C="S" THEN STOP
         ELSE IF C<>"C" THEN GOTO INIT1

READ PBID TO I
IF I<>BRDID THEN ENTRY
        WRITE [1] / "WRONG PERFORMANCE BOARD!" /
        WRITE [1,5(4)]    "BOARD ID NUMBER:  " I /
        WRITE [1,5(4)]    "SHOULD BE:  " BRDID //
        STOP
        EXIT

GO TO CONTINUE

;*************************************
;*   SUBROUTINES FOR INITIALIZATION   *
;*************************************

PIN1:    ; PIN CONNECTIONS FOR FUNCTIONAL TESTS

ROWADD=IN1,NRZB,BCLK1,MUX,<Y8-0,X8-0>
COLADD=IN1,NRZB,BCLK2,<X8-0>
RAS=IN1,/RZZ,BCLK3
CAS=IN1,/RZZ,BCLK4
WE=IN1,/RZZ,BCLK5
DQ=IN1,XOR,ACLK1,BCLK6,OUT1,VT1,IL1,STRB1,DRE1,DRERZ,<D3-0>
G=IN1,/RZZ,BCLK7
GOTO CONT

PIN2:    ; PIN CONNECTIONS FOR IOZH/L TESTS
ROWADD=IN1,FIXL
COLADD=IN1,FIXL
RAS=IN1,FIXH
CAS=IN1,FIXH
WE=IN1,FIXH
DQ=OPEN
G=IN1,FIXH
GOTO CONT

VIN1:    ; NOMINAL LEVELS FOR FUNCTIONAL TEST

VS1=5.0V
IN1=3.0V,0.0V
OUT1=2.0V,1.0V
IL1=-1MA,1MA
VT1=1.5V
GOTO CONT

VIN2:    ; NOMINAL SUPPLY VOLTAGE FOR FUNCTIONAL TEST

VS1=5V
IN1=2.4V,0.7V
OUT1=2.4V,0.4V
IL1=-1MA,1MA
VT1=1.5V
GOTO CONT

VIN3:    ; MAXIMUM SUPPLY VOLTAGE FOR FUNCTIONAL TEST

VS1=5.5V
IN1=2.4V,0.7V
```

```
OUT1=2.4V,0.4V
IL1=-1MA,1MA
VT1=1.5V
GOTO CONT

VIN4:    ; MINIMUM SUPPLY VOLTAGE FOR FUNCTIONAL/SPEED TEST

VS1=4.5V
IN1=4.5V,0V
OUT1=1.5V,1.5V
IL1=-1MA,1MA
VT1=1.5V
GOTO CONT

VIN5:    ; NOMINAL SUPPLY VOLTAGE FOR FUNCTIONAL/SPEED TEST

VS1=5.0V
IN1=5.0V,0V
OUT1=1.5V,1.5V
IL1=-1MA,1MA
VT1=1.5V
GOTO CONT

VIN6:    ; MAXIMUM SUPPLY VOLTAGE FOR FUNCTIONAL/SPEED TEST

VS1=5.5V
IN1=5.5V,0V
OUT1=1.5V,1.5V
IL1=-1MA,1MA
VT1=1.5V
GOTO CONT

VIN7:    ; NOMINAL SUPPLY VOLTAGE FOR ACCESS TIME TEST

VS1=5V
IN1=5.0V,0V
OUT1=3.0V,0.4V
IL1=-1MA,1MA
VT1=1.5V
GOTO CONT

VIN8:    ; NOMINAL SUPPLY VOLTAGE FOR FUNCTIONAL TEST

VS1=5V
IN1=5.0V,0V
OUT1=2.4V,0.4V
IL1=-1MA,1MA
VT1=1.5V
GOTO CONT

REF1:    ; POWER ON SEQUENCE FOR ALL TESTS
TIME2=10MS : VS1                ;VCC
TIME3=1MS : OTHERS
GOTO CONT

TIM1:    ; LOWERED TO 500KHZ TO COMPENSATE FOR LONG WIRING

RATE=    2000NS  ;500KHZ

BCLK1=   100NS     ;ROW ADDRESS
```

```
CCLK1=  400NS

BCLK2=  700NS    ;COL ADDRESS
CCLK2=  1000NS

BCLK3=  200NS     ;RAS
CCLK3=  1400NS

BCLK4=  800NS    ;CAS
CCLK4=  1200NS

BCLK5=  900NS    ;WE
CCLK5=  1200NS

ACLK1=  0NS      ;DQ
BCLK6=  800NS
CCLK6=  1100NS
STRB1=  1200NS
DREL1=  0NS
DRET1=  1150NS

BCLK7=  750NS    ;G
CCLK7=  1500NS

GOTO CONT

;TIM1:    ; RELAXED TIMINGS FOR FUNCTIONAL TESTS

;RATE=    400NS  ;2.5MHZ

;BCLK1=  20NS     ;ROW ADDRESS
;CCLK1=  80NS

;BCLK2=  140NS    ;COL ADDRESS
;CCLK2=  200NS

;BCLK3=  40NS     ;RAS
;CCLK3=  280NS

;BCLK4=  160NS    ;CAS
;CCLK4=  240NS

;BCLK5=  180NS    ;WE
;CCLK5=  240NS

;ACLK1=  0NS      ;DQ
;BCLK6=  160NS
;CCLK6=  220NS
;STRB1=  240NS
;DREL1=  0NS
;DRET1=  230NS

;BCLK7= 150NS    ;G
;CCLK7= 300NS

;GOTO CONT

TIM2:    ; TIMINGS FOR FUNCTIONAL/SPEED TESTS

RATE=    200NS
```

```
BCLK1=  10NS    ;ROW ADDRESS
CCLK1=  40NS

BCLK2=  70NS    ;COL ADDRESS
CCLK2=  100NS

BCLK3=  20NS    ;RAS
CCLK3=  140NS

BCLK4=  80NS    ;CAS
CCLK4=  120NS

BCLK5=  90NS    ;WE
CCLK5=  120NS

ACLK1=  0NS     ;DQ
BCLK6=  80NS
CCLK6=  110NS
STRB1=  120NS
DREL1=  0NS
DRET1=  230NS
GOTO CONT

MENU:

        WRITE [1],/,"DYNAMIC TEST MENU"
        WRITE [1],/,"-----------------"
        WRITE [1],/,"    1 = DRAM 1A"
        WRITE [1],/,"    2 = DRAM 2A"
        WRITE [1],/,"    3 = DRAM 3A"
        WRITE [1],/,"    4 = DRAM 4A"
        WRITE [1],/,"    5 = DRAM 5A"
        WRITE [1],/,"    6 = DRAM 6A"
        WRITE [1],/,"    7 = DRAM 7A"
        WRITE [1],/,"    8 = DRAM 8A"
        WRITE [1],/,"    9 = DRAM 1B"
        WRITE [1],/,"   10 = DRAM 2B"
        WRITE [1],/,"   11 = DRAM 3B"
        WRITE [1],/,"   12 = DRAM 4B"
        WRITE [1],/,"   13 = DRAM 5B"
        WRITE [1],/,"   14 = DRAM 6B"
        WRITE [1],/,"   15 = DRAM 7B"
        WRITE [1],/,"   16 = EXIT MENU",/

GOTO CONT

GETSEL:

        INPUT [1,7(0)] "YOUR CHOICE? ",SEL

        IF SEL<0 OR SEL>16 THEN SEL=17

GOTO CONT

END
```

```
SOCKET PINS ;  for STACKED MEMORY MODULE
;PIN=CHANNEL            PIN
P1=133=CAS5B    ;
P2=134=CAS6B    ;
P3=135=CAS7B    ;
P4=136=CAS8B    ;
P5=73=A1        ; MUX ON 74
P6=75=A3        ; MUX ON 76
;P7=137=N/C     ;
P8=139=A5       ; MUX ON 140
P9=14=RAS8B     ;
P10=142=RAS7B   ;
P11=143=RAS6B   ;
P12=144=RAS5B   ;
;P13=0=VSS      ;
P14=145=CAS5A   ;
P15=146=CAS6A   ;
P16=147=CAS7A   ;
P17=148=CAS8A   ;
P18=21=A7       ; MUX ON 22
P19=23=G        ;
P20=149=DQ4     ;
P21=150=DQ2     ;
P22=28=RAS8A    ;
P23=27=RAS7A    ;
P24=26=RAS6A    ;
P25=25=RAS5A    ;
P26=168=RAS4A   ;
P27=167=RAS3A   ;
P28=166=RAS2A   ;
P29=165=RAS1A   ;
P30=42=DQ1      ;
P31=41=DQ3      ;
P32=47=A8       ; MUX ON 48
P33=45=WE       ;
P34=176=CAS1A   ;
P35=175=CAS2A   ;
P36=174=CAS3A   ;
P37=173=CAS4A   ;
;P38=0=VCC      ;
P39=180=RAS4B   ;
P40=179=RAS3B   ;
```

```
P41=178=RAS2B    ;
P42=177=RAS1B    ;
P43=55=A6        ; MUX ON 56
P44=53=A4        ; MUX ON 54
P45=183=A0       ; MUX ON 184
P46=181=A2       ; MUX ON 182
P47=188=CAS1B    ;
P48=187=CAS2B    ;
P49=186=CAS3B    ;
P50=185=CAS4B    ;
P51=184=A0M      ;
P52=74=A1M       ;
P53=182=A2M      ;
P54=76=A3M       ;
P55=54=A4M       ;
P56=140=A5M      ;
P57=56=A6M       ;
P58=22=A7M       ;
P59=48=A8M       ;

END
```

```
LPAT MATS   PINS ; FUNCTIONAL FOR 256K X 1 X 16 DRAM, 8MS REFRESH

DEFINE D1MX1

COMMON INIT,RAS,@
      RS1A,RS2A,RS3A,RS4A,RS5A,RS6A,RS7A,RS8A,@
      RS1B,RS2B,RS3B,RS4B,RS5B,RS6B,RS7B,RS8B,@
      RD1A,RD2A,RD3A,RD4A,RD5A,RD6A,RD7A,RD8A,@
      RD1B,RD2B,RD3B,RD4B,RD5B,RD6B,RD7B,RD8B,@
      WR1A,WR2A,WR3A,WR4A,WR5A,WR6A,WR7A,WR8A,@
      WR1B,WR2B,WR3B,WR4B,WR5B,WR6B,WR7B,WR8B

CHANNEL 33,19,@
      29,34,28,35,27,36,26,37,25,14,24,15,23,16,22,17,@
      42,47,41,48,40,49,39,50,12,1,11,2,10,3,9,4,@
      32,59,18,58,43,57,8,56,44,55,6,54,46,53,5,52,45,51,@
      20,31,21,30

PFDEF

FIELD ALL<33,19,29,34,28,35,27,36,26,37,25,14,24,15,23,16,22,17,@
       42,47,41,48,40,49,39,50,12,1,11,2,10,3,9,4,@
       32,59,18,58,43,57,8,56,44,55,6,54,46,53,5,52,45,51,@
       20,31,21,30>

;        RCRCRCRCRCRCRCRCRCRCRCRCRCRC
;        AAAAAAAAAAAAAAAAAAAAAAAAAAAAAA A A A A A A A A
;        SSSSSSSSSSSSSSSSSSSSSSSSSSSSSS8 7 6 5 4 3 2 1 0 DDDD
;      W 11223344556677881122334455667788 A A A A A A A A AQQQQ
;      EGAAAAAAAAAAAAAAAABBBBBBBBBBBBBBB 8 7 6 5 4 3 2 1 04321

INIT = 11111111111111111111111111111111000000000000000000XXXX
RD1A = 10001111111111111111111111111111000000000000000000LLLL
RD2A = 10110011111111111111111111111111000000000000000000LLLL
RD3A = 10111100111111111111111111111111000000000000000000LLLL
RD4A = 10111111001111111111111111111111000000000000000000LLLL
RD5A = 10111111110011111111111111111111000000000000000000LLLL
RD6A = 10111111111100111111111111111111000000000000000000LLLL
RD7A = 10111111111111001111111111111111000000000000000000LLLL
RD8A = 10111111111111110011111111111111000000000000000000LLLL
RD1B = 10111111111111111100111111111111000000000000000000LLLL
RD2B = 10111111111111111111001111111111000000000000000000LLLL
RD3B = 10111111111111111111110011111111000000000000000000LLLL
RD4B = 10111111111111111111111100111111000000000000000000LLLL
RD5B = 10111111111111111111111111001111000000000000000000LLLL
RD6B = 10111111111111111111111111110011000000000000000000LLLL
```

```
RD7B = 10111111111111111111111111111100110000000000000000000LLLL
RD8B = 10111111111111111111111111111110000000000000000000000LLLL
WR1A = 01001111111111111111111111111111110000000000000000000000
WR2A = 01110011111111111111111111111111110000000000000000000000
WR3A = 01111100111111111111111111111111110000000000000000000000
WR4A = 01111111001111111111111111111111110000000000000000000000
WR5A = 01111111110011111111111111111111110000000000000000000000
WR6A = 01111111111100111111111111111111110000000000000000000000
WR7A = 01111111111111001111111111111111110000000000000000000000
WR8A = 01111111111111110011111111111111110000000000000000000000
WR1B = 01111111111111111100111111111111110000000000000000000000
WR2B = 01111111111111111111001111111111110000000000000000000000
WR3B = 01111111111111111111110011111111110000000000000000000000
WR4B = 01111111111111111111111100111111110000000000000000000000
WR5B = 01111111111111111111111111001111110000000000000000000000
WR6B = 01111111111111111111111111110011110000000000000000000000
WR7B = 01111111111111111111111111111100110000000000000000000000
WR8B = 01111111111111111111111111111111000000000000000000000000
RS1A = 11011111111111111111111111111111110000000000000000000XXXX
RS2A = 11111011111111111111111111111111110000000000000000000XXXX
RS3A = 11111101111111111111111111111111110000000000000000000XXXX
RS4A = 11111111011111111111111111111111110000000000000000000XXXX
RS5A = 11111111101111111111111111111111110000000000000000000XXXX
RS6A = 11111111111011111111111111111111110000000000000000000XXXX
RS7A = 11111111111110111111111111111111110000000000000000000XXXX
RS8A = 11111111111111101111111111111111110000000000000000000XXXX
RS1B = 11111111111111111011111111111111110000000000000000000XXXX
RS2B = 11111111111111111110111111111111110000000000000000000XXXX
RS3B = 11111111111111111111011111111111110000000000000000000XXXX
RS4B = 11111111111111111111101111111111110000000000000000000XXXX
RS5B = 11111111111111111111110111111111110000000000000000000XXXX
RS6B = 11111111111111111111111011111111110000000000000000000XXXX
RS7B = 11111111111111111111111101111111110000000000000000000XXXX
RS8B = 11111111111111111111111110111111110000000000000000000XXXX
 RAS = 11010101010101010101010101010101010000000000000000000XXXX

DEFINE END

MODE ALPG,MUX,REFRESH 512

REGISTER

      XMAX=#1FF  ;9 Row Address Bits
      YMAX=#1FF  ;9 Column Address Bits
      LMAX=#1FF
      HMAX=#1FF
```

```
      TPH=#0          ;Data register initializer
      IDX1=#1FE  ;Inner Address loop counter
      IDX2=#1FF  ;Outer Address loop counter
      IDX3=#1         ;Loop counter for inverting data
      IDX4=#8         ;Wakeup cycle counter
      RIDX=#1FF  ;Refresh cycle counter
      SPI=#20         ;Address of refresh cycle
      TIMER=8MS  ;Refresh interval

SDEF  ACLR = XB<0 XC<0 YB<0 YC<0 X<XB Y<YB
SDEF TPCLR = TP<TPH
SDEF  AINC = XB<XB+1 YB<YB+1^BX  X<XB Y<YB
SDEF  ADEC = XB<XB-1 YB<YB-1^BX  X<XB Y<YB
SDEF TPCMP = TP</TP
SDEF  SAVE = XC<XB YC<YB
SDEF  SEND = XC<XC YC<YC    X<XC Y<YC
SDEF   ONE = XC<XB-1 YC<YB
SDEF   TWO = XC<XB YC<YB+1
SDEF THREE = XC<XB+1 YC<YB
SDEF  FOUR = XC<XB YC<YB-1
SDEF   REF = RF<RF+1        X<RF Y<YB

CFPF

LOC #0  ;ICC ALL ZEROS

      NOP        TPCLR ACLR  !'INIT
      IDX2              ACLR  !'RAS
      IDX1       FP0   AINC  !'WR1A
      LDI1       FP0   AINC  !'WR1A
      IDX1       FP0   AINC  !'WR1A
      JNI   .-1  FP0   AINC  !'WR1A

LOC #10  ;ICC ALL ONES

      NOP        TPCLR ACLR  !'INIT
      IDX2              ACLR  !'RAS
      IDX1       FP0   AINC  /D!'WR1A
      LDI1       FP0   AINC  /D!'WR1A
      IDX1       FP0   AINC  /D!'WR1A
      JNI   .-1  FP0   AINC  /D!'WR1A

LOC #20  ;REFRESH

      NOP               REF   !'RAS
```

```
LOC #50  ;MATS++ MARCH ALGORITHM

     NOP         TPCLR ACLR  !'INIT
     IDX4              ACLR  !'RAS ;Wakeup

;BEGIN WITH DRAM #1A
                                    ; M1: ^(W0)
     LDI2                     !'INIT     ;Load outer loop counter
     IDX1                AINC !'WR1A     ;Inner loop
     JNI   .-1           AINC !'WR1A     ;Outer loop
                                    ; M2: ^(R0,W1)
     LDI2                ACLR !'INIT
     LDI2                     !'INIT
     NOP                      !'RD1A
     JNI   .-1   /D      AINC !'WR1A
     JNI   .-3                !'INIT
                                    ; M3: v(R1,W0,R0)
     LDI2                ADEC !'INIT
     LDI2                     !'INIT
     NOP         /D           !'RD1A
     NOP                      !'WR1A
     JNI   .-2           AINC !'RD1A
     JNI   .-4                !'INIT

;REPEAT WITH DRAM #2A
                                    ; M1: ^(W0)
     LDI2                     !'INIT
     IDX1                AINC !'WR2A
     JNI   .-1           AINC !'WR2A
                                    ; M2: ^(R0,W1)
     LDI2                ACLR !'INIT
     LDI2                     !'INIT
     NOP                      !'RD2A
     JNI   .-1   /D      AINC !'WR2A
     JNI   .-3                !'INIT
                                    ; M3: v(R1,W0,R0)
     LDI2                ADEC !'INIT
     LDI2                     !'INIT
     NOP         /D           !'RD2A
     NOP                      !'WR2A
     JNI   .-2           AINC !'RD2A
     JNI   .-4                !'INIT

;REPEAT WITH DRAM #3A
                                    ; M1: ^(W0)
```

```
      LDI2                    !'INIT
      IDX1              AINC  !'WR3A
      JNI   .-1         AINC  !'WR3A
                                    ; M2: ^(R0,W1)
      LDI2              ACLR  !'INIT
      LDI2                    !'INIT
      NOP                     !'RD3A
      JNI   .-1   /D    AINC  !'WR3A
      JNI   .-3               !'INIT
                                    ; M3: v(R1,W0,R0)
      LDI2              ADEC  !'INIT
      LDI2                    !'INIT
      NOP         /D          !'RD3A
      NOP                     !'WR3A
      JNI   .-2         AINC  !'RD3A
      JNI   .-4               !'INIT

;REPEAT WITH DRAM #4A
                                    ; M1: ^(W0)
      LDI2                    !'INIT
      IDX1              AINC  !'WR4A
      JNI   .-1         AINC  !'WR4A
                                    ; M2: ^(R0,W1)
      LDI2              ACLR  !'INIT
      LDI2                    !'INIT
      NOP                     !'RD4A
      JNI   .-1   /D    AINC  !'WR4A
      JNI   .-3               !'INIT
                                    ; M3: v(R1,W0,R0)
      LDI2              ADEC  !'INIT
      LDI2                    !'INIT
      NOP         /D          !'RD4A
      NOP                     !'WR4A
      JNI   .-2         AINC  !'RD4A
      JNI   .-4               !'INIT

;REPEAT WITH DRAM #5A
                                    ; M1: ^(W0)
      LDI2                    !'INIT
      IDX1              AINC  !'WR5A
      JNI   .-1         AINC  !'WR5A
                                    ; M2: ^(R0,W1)
      LDI2              ACLR  !'INIT
      LDI2                    !'INIT
      NOP                     !'RD5A
      JNI   .-1   /D    AINC  !'WR5A
```

```
      JNI   .-3                !'INIT
                                     ; M3: v(R1,W0,R0)
      LDI2              ADEC   !'INIT
      LDI2                     !'INIT
      NOP         /D           !'RD5A
      NOP                      !'WR5A
      JNI   .-2         AINC   !'RD5A
      JNI   .-4                !'INIT

;REPEAT WITH DRAM #6A
                                     ; M1: ^(W0)
      LDI2                     !'INIT
      IDX1              AINC   !'WR6A
      JNI   .-1         AINC   !'WR6A
                                     ; M2: ^(R0,W1)
      LDI2              ACLR   !'INIT
      LDI2                     !'INIT
      NOP                      !'RD6A
      JNI   .-1   /D    AINC   !'WR6A
      JNI   .-3                !'INIT
                                     ; M3: v(R1,W0,R0)
      LDI2              ADEC   !'INIT
      LDI2                     !'INIT
      NOP         /D           !'RD6A
      NOP                      !'WR6A
      JNI   .-2         AINC   !'RD6A
      JNI   .-4                !'INIT

;REPEAT WITH DRAM #7A
                                     ; M1: ^(W0)
      LDI2                     !'INIT
      IDX1              AINC   !'WR7A
      JNI   .-1         AINC   !'WR7A
                                     ; M2: ^(R0,W1)
      LDI2              ACLR   !'INIT
      LDI2                     !'INIT
      NOP                      !'RD7A
      JNI   .-1   /D    AINC   !'WR7A
      JNI   .-3                !'INIT
                                     ; M3: v(R1,W0,R0)
      LDI2              ADEC   !'INIT
      LDI2                     !'INIT
      NOP         /D           !'RD7A
      NOP                      !'WR7A
      JNI   .-2         AINC   !'RD7A
      JNI   .-4                !'INIT
```

```
;REPEAT WITH DRAM #8A
                                        ; M1: ^(W0)
      LDI2                        !'INIT
      IDX1              AINC      !'WR8A
      JNI   .-1         AINC      !'WR8A
                                        ; M2: ^(R0,W1)
      LDI2              ACLR      !'INIT
      LDI2                        !'INIT
      NOP                         !'RD8A
      JNI   .-1   /D    AINC      !'WR8A
      JNI   .-3                   !'INIT
                                        ; M3: v(R1,W0,R0)
      LDI2              ADEC      !'INIT
      LDI2                        !'INIT
      NOP         /D              !'RD8A
      NOP                         !'WR8A
      JNI   .-2         AINC      !'RD8A
      JNI   .-4                   !'INIT

;REPEAT WITH DRAM #1B
                                        ; M1: ^(W0)
      LDI2                        !'INIT
      IDX1              AINC      !'WR1B
      JNI   .-1         AINC      !'WR1B
                                        ; M2: ^(R0,W1)
      LDI2              ACLR      !'INIT
      LDI2                        !'INIT
      NOP                         !'RD1B
      JNI   .-1   /D    AINC      !'WR1B
      JNI   .-3                   !'INIT
                                        ; M3: v(R1,W0,R0)
      LDI2              ADEC      !'INIT
      LDI2                        !'INIT
      NOP         /D              !'RD1B
      NOP                         !'WR1B
      JNI   .-2         AINC      !'RD1B
      JNI   .-4                   !'INIT

;REPEAT WITH DRAM #2B
                                        ; M1: ^(W0)
      LDI2                        !'INIT
      IDX1              AINC      !'WR2B
      JNI   .-1         AINC      !'WR2B
                                        ; M2: ^(R0,W1)
      LDI2              ACLR      !'INIT
```

```
      LDI2                    !'INIT
      NOP                     !'RD2B
      JNI   .-1   /D    AINC  !'WR2B
      JNI   .-3               !'INIT
                                    ; M3: v(R1,W0,R0)
      LDI2              ADEC  !'INIT
      LDI2                    !'INIT
      NOP         /D          !'RD2B
      NOP                     !'WR2B
      JNI   .-2         AINC  !'RD2B
      JNI   .-4               !'INIT

;REPEAT WITH DRAM #3B
                                    ; M1: ^(W0)
      LDI2                    !'INIT
      IDX1              AINC  !'WR3B
      JNI   .-1         AINC  !'WR3B
                                    ; M2: ^(R0,W1)
      LDI2              ACLR  !'INIT
      LDI2                    !'INIT
      NOP                     !'RD3B
      JNI   .-1   /D    AINC  !'WR3B
      JNI   .-3               !'INIT
                                    ; M3: v(R1,W0,R0)
      LDI2              ADEC  !'INIT
      LDI2                    !'INIT
      NOP         /D          !'RD3B
      NOP                     !'WR3B
      JNI   .-2         AINC  !'RD3B
      JNI   .-4               !'INIT

;REPEAT WITH DRAM #4B
                                    ; M1: ^(W0)
      LDI2                    !'INIT
      IDX1              AINC  !'WR4B
      JNI   .-1         AINC  !'WR4B
                                    ; M2: ^(R0,W1)
      LDI2              ACLR  !'INIT
      LDI2                    !'INIT
      NOP                     !'RD4B
      JNI   .-1   /D    AINC  !'WR4B
      JNI   .-3               !'INIT
                                    ; M3: v(R1,W0,R0)
      LDI2              ADEC  !'INIT
      LDI2                    !'INIT
      NOP         /D          !'RD4B
```

```
      NOP                        !'WR4B
      JNI   .-2           AINC   !'RD4B
      JNI   .-4                  !'INIT

;REPEAT WITH DRAM #5B
                                 ; M1: ^(W0)
      LDI2                       !'INIT
      IDX1                AINC   !'WR5B
      JNI   .-1           AINC   !'WR5B
                                 ; M2: ^(R0,W1)
      LDI2                ACLR   !'INIT
      LDI2                       !'INIT
      NOP                        !'RD5B
      JNI   .-1   /D      AINC   !'WR5B
      JNI   .-3                  !'INIT
                                 ; M3: v(R1,W0,R0)
      LDI2                ADEC   !'INIT
      LDI2                       !'INIT
      NOP           /D           !'RD5B
      NOP                        !'WR5B
      JNI   .-2           AINC   !'RD5B
      JNI   .-4                  !'INIT

;REPEAT WITH DRAM #6B
                                 ; M1: ^(W0)
      LDI2                       !'INIT
      IDX1                AINC   !'WR6B
      JNI   .-1           AINC   !'WR6B
                                 ; M2: ^(R0,W1)
      LDI2                ACLR   !'INIT
      LDI2                       !'INIT
      NOP                        !'RD6B
      JNI   .-1   /D      AINC   !'WR6B
      JNI   .-3                  !'INIT
                                 ; M3: v(R1,W0,R0)
      LDI2                ADEC   !'INIT
      LDI2                       !'INIT
      NOP           /D           !'RD6B
      NOP                        !'WR6B
      JNI   .-2           AINC   !'RD6B
      JNI   .-4                  !'INIT

;REPEAT WITH DRAM #7B
                                 ; M1: ^(W0)
      LDI2                       !'INIT
      IDX1                AINC   !'WR7B
```

```
      JNI   .-1          AINC  !'WR7B
                                     ; M2: ^(R0,W1)
      LDI2               ACLR  !'INIT
      LDI2                     !'INIT
      NOP                      !'RD7B
      JNI   .-1    /D    AINC  !'WR7B
      JNI   .-3                !'INIT
                                     ; M3: v(R1,W0,R0)
      LDI2               ADEC  !'INIT
      LDI2                     !'INIT
      NOP          /D          !'RD7B
      NOP                      !'WR7B
      JNI   .-2          AINC  !'RD7B
      JNI   .-4                !'INIT

LOC #150  ;MATS++ MARCH ALGORITHM

      NOP          TPCLR ACLR  !'INIT
      IDX4               ACLR  !'RAS ;Wakeup

;BEGIN WITH DRAM #1A
                                     ; M1: ^(W0)
      LDI2                     !'INIT     ;Load outer loop counter
      IDX1               AINC  !'WR1A     ;Inner loop
      JNI   .-1          AINC  !'WR1A     ;Outer loop

                                     ; M2: ^(R0,W1)
      LDI2               ACLR  !'INIT
      LDI2                     !'INIT
      NOP                      !'RD1A
      JNI   .-1    /D    AINC  !'WR1A
      JNI   .-3                !'INIT
                                     ; M3: v(R1,W0,R0)
      LDI2               ADEC  !'INIT
      LDI2                     !'INIT
      NOP          /D          !'RD1A
      NOP                      !'WR1A
      JNI   .-2          AINC  !'RD1A
      JNI   .-4                !'INIT

;REPEAT WITH DRAM #2A

      NOP          TPCLR ACLR  !'INIT
      IDX4               ACLR  !'RAS ;Wakeup
                                     ; M1: ^(W0)
      LDI2                     !'INIT
```

```
      IDX1              AINC  !'WR2A
      JNI   .-1         AINC  !'WR2A
                                ; M2: ^(R0,W1)
      LDI2              ACLR  !'INIT
      LDI2                    !'INIT
      NOP                     !'RD2A
      JNI   .-1   /D    AINC  !'WR2A
      JNI   .-3               !'INIT
                                ; M3: v(R1,W0,R0)
      LDI2              ADEC  !'INIT
      LDI2                    !'INIT
      NOP         /D          !'RD2A
      NOP                     !'WR2A
      JNI   .-2         AINC  !'RD2A
      JNI   .-4               !'INIT

;REPEAT WITH DRAM #3A

      NOP         TPCLR ACLR  !'INIT
      IDX4              ACLR  !'RAS ;Wakeup
                                ; M1: ^(W0)
      LDI2                    !'INIT
      IDX1              AINC  !'WR3A
      JNI   .-1         AINC  !'WR3A
                                ; M2: ^(R0,W1)
      LDI2              ACLR  !'INIT
      LDI2                    !'INIT
      NOP                     !'RD3A
      JNI   .-1   /D    AINC  !'WR3A
      JNI   .-3               !'INIT
                                ; M3: v(R1,W0,R0)
      LDI2              ADEC  !'INIT
      LDI2                    !'INIT
      NOP         /D          !'RD3A
      NOP                     !'WR3A
      JNI   .-2         AINC  !'RD3A
      JNI   .-4               !'INIT

;REPEAT WITH DRAM #4A

      NOP         TPCLR ACLR  !'INIT
      IDX4              ACLR  !'RAS ;Wakeup
                                ; M1: ^(W0)
      LDI2                    !'INIT
      IDX1              AINC  !'WR4A
      JNI   .-1         AINC  !'WR4A
```

```
                                        ; M2: ^(R0,W1)
      LDI2              ACLR  !'INIT
      LDI2                    !'INIT
      NOP                     !'RD4A
      JNI   .-1   /D    AINC  !'WR4A
      JNI   .-3               !'INIT
                                        ; M3: v(R1,W0,R0)
      LDI2              ADEC  !'INIT
      LDI2                    !'INIT
      NOP         /D          !'RD4A
      NOP                     !'WR4A
      JNI   .-2         AINC  !'RD4A
      JNI   .-4               !'INIT

;REPEAT WITH DRAM #5A

      NOP         TPCLR ACLR  !'INIT
      IDX4              ACLR  !'RAS ;Wakeup
                                        ; M1: ^(W0)
      LDI2                    !'INIT
      IDX1              AINC  !'WR5A
      JNI   .-1         AINC  !'WR5A
                                        ; M2: ^(R0,W1)
      LDI2              ACLR  !'INIT
      LDI2                    !'INIT
      NOP                     !'RD5A
      JNI   .-1   /D    AINC  !'WR5A
      JNI   .-3               !'INIT
                                        ; M3: v(R1,W0,R0)
      LDI2              ADEC  !'INIT
      LDI2                    !'INIT
      NOP         /D          !'RD5A
      NOP                     !'WR5A
      JNI   .-2         AINC  !'RD5A
      JNI   .-4               !'INIT

;REPEAT WITH DRAM #6A

      NOP         TPCLR ACLR  !'INIT
      IDX4              ACLR  !'RAS ;Wakeup
                                        ; M1: ^(W0)
      LDI2                    !'INIT
      IDX1              AINC  !'WR6A
      JNI   .-1         AINC  !'WR6A
                                        ; M2: ^(R0,W1)
      LDI2              ACLR  !'INIT
```

```
      LDI2                    !'INIT
      NOP                     !'RD6A
      JNI   .-1   /D    AINC  !'WR6A
      JNI   .-3               !'INIT
                                   ; M3: v(R1,W0,R0)
      LDI2              ADEC  !'INIT
      LDI2                    !'INIT
      NOP         /D          !'RD6A
      NOP                     !'WR6A
      JNI   .-2         AINC  !'RD6A
      JNI   .-4               !'INIT

;REPEAT WITH DRAM #7A

      NOP         TPCLR ACLR  !'INIT
      IDX4              ACLR  !'RAS ;Wakeup
                                   ; M1: ^(W0)
      LDI2                    !'INIT
      IDX1              AINC  !'WR7A
      JNI   .-1         AINC  !'WR7A
                                   ; M2: ^(R0,W1)
      LDI2              ACLR  !'INIT
      LDI2                    !'INIT
      NOP                     !'RD7A
      JNI   .-1   /D    AINC  !'WR7A
      JNI   .-3               !'INIT
                                   ; M3: v(R1,W0,R0)
      LDI2              ADEC  !'INIT
      LDI2                    !'INIT
      NOP         /D          !'RD7A
      NOP                     !'WR7A
      JNI   .-2         AINC  !'RD7A
      JNI   .-4               !'INIT

;REPEAT WITH DRAM #8A

      NOP         TPCLR ACLR  !'INIT
      IDX4              ACLR  !'RAS ;Wakeup
                                   ; M1: ^(W0)
      LDI2                    !'INIT
      IDX1              AINC  !'WR8A
      JNI   .-1         AINC  !'WR8A
                                   ; M2: ^(R0,W1)
      LDI2              ACLR  !'INIT
      LDI2                    !'INIT
      NOP                     !'RD8A
```

```
      JNI   .-1   /D    AINC  !'WR8A
      JNI   .-3           !'INIT
                                ; M3: v(R1,W0,R0)
      LDI2              ADEC  !'INIT
      LDI2                    !'INIT
      NOP         /D          !'RD8A
      NOP                     !'WR8A
      JNI   .-2         AINC  !'RD8A
      JNI   .-4               !'INIT

;REPEAT WITH DRAM #1B

      NOP         TPCLR ACLR  !'INIT
      IDX4              ACLR  !'RAS ;Wakeup
                                ; M1: ^(W0)
      LDI2                    !'INIT
      IDX1              AINC  !'WR1B
      JNI   .-1         AINC  !'WR1B
                                ; M2: ^(R0,W1)
      LDI2              ACLR  !'INIT
      LDI2                    !'INIT
      NOP                     !'RD1B
      JNI   .-1   /D    AINC  !'WR1B
      JNI   .-3               !'INIT
                                ; M3: v(R1,W0,R0)
      LDI2              ADEC  !'INIT
      LDI2                    !'INIT
      NOP         /D          !'RD1B
      NOP                     !'WR1B
      JNI   .-2         AINC  !'RD1B
      JNI   .-4               !'INIT

;REPEAT WITH DRAM #2B

      NOP         TPCLR ACLR  !'INIT
      IDX4              ACLR  !'RAS ;Wakeup
                                ; M1: ^(W0)
      LDI2                    !'INIT
      IDX1              AINC  !'WR2B
      JNI   .-1         AINC  !'WR2B
                                ; M2: ^(R0,W1)
      LDI2              ACLR  !'INIT
      LDI2                    !'INIT
      NOP                     !'RD2B
      JNI   .-1   /D    AINC  !'WR2B
      JNI   .-3               !'INIT
```

```
                                        ; M3: v(R1,W0,R0)
      LDI2              ADEC  !'INIT
      LDI2                    !'INIT
      NOP         /D          !'RD2B
      NOP                     !'WR2B
      JNI   .-2         AINC  !'RD2B
      JNI   .-4               !'INIT

;REPEAT WITH DRAM #3B

      NOP         TPCLR ACLR  !'INIT
      IDX4              ACLR  !'RAS ;Wakeup
                                        ; M1: ^(W0)
      LDI2                    !'INIT
      IDX1              AINC  !'WR3B
      JNI   .-1         AINC  !'WR3B
                                        ; M2: ^(R0,W1)
      LDI2              ACLR  !'INIT
      LDI2                    !'INIT
      NOP                     !'RD3B
      JNI   .-1   /D    AINC  !'WR3B
      JNI   .-3               !'INIT
                                        ; M3: v(R1,W0,R0)
      LDI2              ADEC  !'INIT
      LDI2                    !'INIT
      NOP         /D          !'RD3B
      NOP                     !'WR3B
      JNI   .-2         AINC  !'RD3B
      JNI   .-4               !'INIT

;REPEAT WITH DRAM #4B

      NOP         TPCLR ACLR  !'INIT
      IDX4              ACLR  !'RAS ;Wakeup
                                        ; M1: ^(W0)
      LDI2                    !'INIT
      IDX1              AINC  !'WR4B
      JNI   .-1         AINC  !'WR4B
                                        ; M2: ^(R0,W1)
      LDI2              ACLR  !'INIT
      LDI2                    !'INIT
      NOP                     !'RD4B
      JNI   .-1   /D    AINC  !'WR4B
      JNI   .-3               !'INIT
                                        ; M3: v(R1,W0,R0)
      LDI2              ADEC  !'INIT
```

```
      LDI2                    !'INIT
      NOP         /D          !'RD4B
      NOP                     !'WR4B
      JNI   .-2         AINC  !'RD4B
      JNI   .-4               !'INIT

;REPEAT WITH DRAM #5B

      NOP         TPCLR ACLR  !'INIT
      IDX4              ACLR  !'RAS ;Wakeup
                                    ; M1: ^(W0)
      LDI2                    !'INIT
      IDX1              AINC  !'WR5B
      JNI   .-1         AINC  !'WR5B
                                    ; M2: ^(R0,W1)
      LDI2              ACLR  !'INIT
      LDI2                    !'INIT
      NOP                     !'RD5B
      JNI   .-1   /D    AINC  !'WR5B
      JNI   .-3               !'INIT
                                    ; M3: v(R1,W0,R0)
      LDI2              ADEC  !'INIT
      LDI2                    !'INIT
      NOP         /D          !'RD5B
      NOP                     !'WR5B
      JNI   .-2         AINC  !'RD5B
      JNI   .-4               !'INIT

;REPEAT WITH DRAM #6B

      NOP         TPCLR ACLR  !'INIT
      IDX4              ACLR  !'RAS ;Wakeup
                                    ; M1: ^(W0)
      LDI2                    !'INIT
      IDX1              AINC  !'WR6B
      JNI   .-1         AINC  !'WR6B
                                    ; M2: ^(R0,W1)
      LDI2              ACLR  !'INIT
      LDI2                    !'INIT
      NOP                     !'RD6B
      JNI   .-1   /D    AINC  !'WR6B
      JNI   .-3               !'INIT
                                    ; M3: v(R1,W0,R0)
      LDI2              ADEC  !'INIT
      LDI2                    !'INIT
      NOP         /D          !'RD6B
```

```
      NOP                        !'WR6B
      JNI   .-2           AINC   !'RD6B
      JNI   .-4                  !'INIT

;REPEAT WITH DRAM #7B

      NOP         TPCLR  ACLR    !'INIT
      IDX4               ACLR    !'RAS ;Wakeup
                                        ; M1: ^(W0)
      LDI2                       !'INIT
      IDX1               AINC    !'WR7B
      JNI   .-1          AINC    !'WR7B
                                        ; M2: ^(R0,W1)
      LDI2               ACLR    !'INIT
      LDI2                       !'INIT
      NOP                        !'RD7B
      JNI   .-1   /D     AINC    !'WR7B
      JNI   .-3                  !'INIT
                                        ; M3: v(R1,W0,R0)
      LDI2               ADEC    !'INIT
      LDI2                       !'INIT
      NOP         /D             !'RD7B
      NOP                        !'WR7B
      JNI   .-2          AINC    !'RD7B
      JNI   .-4                  !'INIT

END
```

Test Article: 3DMM
Test Engineer: Grant Erickson
Test Technician: Matthew Millen
Test Observer:

Date: 9/16/98
Page: 1 of 3

Test Setup Photographs:

Test Part #
Test Sequence #

Interference test on data line #3 (DQ3). Interfering signal inserted through diplexer #2-2 at 1.0ghz.

0 dbm - pass
+10 dbm - pass
+20 dbm - pass
+27 dbm (½w) - Fail
+23 dbm (.2w) - pass
+26 dbm - Fail
+25 dbm (.32w) - pass

Test Article: 3DMM
Test Engineer: Grant Erickson
Test Technician: Matthew Miller
Test Observer:

Date: 9/16/98
Page: 2 of 3

Test Setup Photographs:

Test Part #
Test Sequence #

Interference test on Vcc Line (Pin 38) using high power combiner. Signal is 1MHz Sine wave with signal level measured at output of signal combiner.

1.0 V_{pp} (0.5 V offset) Pass
1.2 V_{pp} (0.6 V offset) Fail

Test Article: 3DMM
Test Engineer: Matthew Miller
Test Technician: Grant Ericksen
Test Observer:

Date: 9/16/98
Page: 3 of 3

Test Setup Photographs:

Test Part #
Test Sequence #

Combined DQ3 & Vcc Test. Tested DQ3 with 1 MHz Interfering Signal.
+29 dbm - pass
+30 dbm - Fail

Reduced interfering signal power on data line DQ3. Increased voltage of 1 MHz interfering signal on Vcc. For "X" power on DQ3 the test failed at "Y" voltage and above on Vcc (but passed at lower value).

DQ3	Vcc	
+29 dbm	2800 mv	(at output of signal combiner)
+28 dbm	900 mv	
+27 dbm	1500 mv	

EMEAP Susceptibility

Test Article: 30MM
Test Engineer: Grant Erickson
Test Technician:
Test Observer:

Date: 9/29/98
Page: 1 of 1

Test Setup Photographs:

Test Part #
Test Sequence #

Test using diplexer

100 KHz	+30.3 dbm	Pass
	+31.3	Fail
200 KHz	+43	Pass
500 KHz	+31.8	Pass
	+32.8	Fail
700 KHz	+43	Pass

Using High Speed Op Amp Combiner

No Signal		Pass
50 KHz	+41	Pass

```
PRO MAIN PINS

;*****************************************************************************
;
;       FILE: MAIN.ASC
;
;*****************************************************************************
;       (C) THE BOEING COMPANY, SEATTLE, WA, 1993
;               BOEING PARTS TEST CENTER
;
;       THE REVISION HISTORY OF THIS PROGRAM CAN BE FOUND IN THE
;       "REVISIONS." FILE LOCATED IN THE SAME DIRECTORY.
;
;*****************************************************************************
;
;  CONTENTS:    TEST PROGRAM FOR THE PROCESSOR MEMORY MODULE MCM
;               THE PACKAGE IS A SMART CARD WITH AN EDGE CONNECTOR
;
;*****************************************************************************

;---------GLOBAL VARIABLES-------------

;DATASET NUMBER
STRING DATASET(35)="NOT RELEASED"

;PART NUMBER
STRING PRTNMBR(25)="PMM MCM"

;PROGRAMMER/AUTHOR
STRING PRGMER(15)="R.K.HOFFMAN"

;RELEASE DATE
STRING RELDATE(15)="NOT RELEASED"

;REQUIREMENTS
STRING REQS(35)="FUNCTIONAL ONLY, MEMORY ONLY"

;LOAD BOARD
STRING LDBRD(15)="PMM"

;LOAD BOARD ID NUMBER - SET WITH ROTARY SWITCHES ON THE PERFORMANCE BOARD
INTEGER BRDID=#0000

;-------- RUN TIME VARIABLES ------------

REAL MAXLIM             ;MAXIMUM LIMIT - FOR OUTPUT ROUTINE
REAL MINLIM             ;MINIMUM LIMIT - FOR OUTPUT ROUTINE
REAL RESULT             ;TEST RESULT - FOR OUTPUT ROUTINE
INTEGER FCNT            ;COUNTER TO HOLD NUMBER OF TESTS THAT FAILED
STRING PF(8)            ;PASS/FAIL STRING - FOR OUTPUT ROUTINE
STRING TSYM(8)          ;TEST SYMBOL - FOR OUTPUT ROUTINE
STRING TCOND(8)         ;TEST CONDITION - FOR OUTPUT ROUTINE
INTEGER SERNUM          ;SERIAL NUMBER OF DUT - FOR OUTPUT ROUTINE
INTEGER LIMCOND         ;FLAG USED IN OUTPUT ROUTINE
STRING FDATE(17)        ;DATE/TIME STRING - USED IN HEADER ROUTINE
INTEGER MINTYP          ;FLAG USED IN OUTPUT ROUTINE
INTEGER MAXTYP          ;FLAG USED IN OUTPUT ROUTINE
INTEGER RCODE           ;FLAG USED IN OUTPUT ROUTINE
INTEGER SFLAG           ;USED TO STORE SFLG VALUE
INTEGER LOOPER          ;USED TO INITIALIZE DO LOOPS
```

```
LOGICAL FHIGH, FMIDD, EXPDATA, INVDATA  ;USED TO CALCULATE EXPECTED DATA VALUES

DIM XPINS(92)            ; ARRAY TO HOLD FAILED PIN NUMBERS
DIM SUSP(92)             ; ARRAY TO INDICATE POSSIBLE PIN PROBLEMS

INTE[2] FCOUNT
LOGI[2] PCOUNT
LOGI[1] STATUS
LOGI[2] DFMADD
LOGI[1] TOFAIL
LOGI[1] STEADD
LOGI[2] DFMFDF
LOGI[2] AFMMEM
LOGI[2] FNDATA
LOGI[2] DFMX
LOGI[2] DFMY
LOGI[1] DFMTSD
LOGI[2] DFMTPD
INTE[2] FADDR

;*****************************************************************************


;#############################################################################
;
;       MAIN PROGRAM
;
;#############################################################################

FCNT = 0        ;INITIALIZE THE FAIL COUNT

;IF INIT KEY HAS BEEN PUNCHED, DISPLAY PROGRAM INFORMATION
IF INIT THEN GOSUB DOINIT

GOSUB DOHEAD
GOSUB DOTESTS
GOSUB DOFOOT
STOP
;#############################################################################
;
;       MAIN TEST ROUTINE
;
;#############################################################################
DOTESTS:
PINLIST DEVPINS=P15-92

PINLIST MABUS=MA16,MA15,MA14,MA13,MA12,MA11,MA10,MA9,MA8,MA7,MA6,MA5,MA4,@
MA3,MA2,MA1,MA0

PINLIST XABUS=MA7,MA6,MA5,MA4,MA3,MA2,MA1,MA0
PINLIST YABUS=MA16,MA15,MA14,MA13,MA12,MA11,MA10,MA9,MA8

PINLIST MPERBUS=MPER23,MPER22,MPER21,MPER20,MPER19,MPER18,MPER17,MPER16,@
MPER15,MPER14,MPER13,MPER12,MPER11,MPER10,MPER9,MPER8,MPER7,MPER6,MPER5,@
MPER4,MPER3,MPER2,MPER1,MPER0

PINLIST U5BUS=MPER0,MPER3,MPER6,MPER9,MPER12,MPER15,MPER18,MPER21

PINLIST U6BUS=MPER1,MPER4,MPER7,MPER10,MPER13,MPER16,MPER19,MPER22
```

```
PINLIST U7BUS=MPER2,MPER5,MPER8,MPER11,MPER14,MPER17,MPER20,MPER23

PINLIST MDBUS=MD31,MD30,MD29,MD28,MD27,MD26,MD25,MD24,MD23,MD22,MD21,MD20,@
MD19,MD18,MD17,MD16,MD15,MD14,MD13,MD12,MD11,MD10,MD9,MD8,MD7,MD6,MD5,MD4,@
MD3,MD2,MD1,MD0

PINLIST POLPINS=MD31,MD30,MD29,MD28,MPER23,MPER22,MPER21

PINLIST U1BUS=MD0,MD4,MD8,MD12,MD16,MD20,MD24,MD28
PINLIST U2BUS=MD1,MD5,MD9,MD13,MD17,MD21,MD25,MD29
PINLIST U3BUS=MD2,MD6,MD10,MD14,MD18,MD22,MD26,MD30
PINLIST U4BUS=MD3,MD7,MD11,MD15,MD19,MD23,MD27,MD31

PINLIST EP4321= MD31,MD27,MD23,MD19,MD15,MD11,MD7,MD3@
                MD30,MD26,MD22,MD18,MD14,MD10,MD6,MD2@
                MD29,MD25,MD21,MD17,MD13,MD9,MD5,MD1@
                MD28,MD24,MD20,MD16,MD12,MD8,MD4,MD0
PINLIST EP765=  MPER23,MPER20,MPER17,MPER14,MPER11,MPER8,MPER5,MPER2@
                MPER22,MPER19,MPER16,MPER13,MPER10,MPER7,MPER4,MPER1@
                MPER21,MPER18,MPER15,MPER12,MPER9,MPER6,MPER3,MPER0

PINLIST CTLPINS=WEIN,CSE,CSS,CSS2,OE

DIM SMA(17)="MA16","MA15","MA14","MA13","MA12","MA11","MA10","MA9","MA8","MA7",@
"MA6","MA5","MA4","MA3","MA2","MA1","MA0"

DIM SMPER(24)="MPER23","MPER22","MPER21","MPER20","MPER19","MPER18","MPER17",@
"MPER16","MPER15","MPER14","MPER13","MPER12","MPER11","MPER10","MPER9","MPER8",@
"MPER7","MPER6","MPER5","MPER4","MPER3","MPER2","MPER1","MPER0"

DIM SMD(32)="MD31","MD30","MD29","MD28","MD27","MD26","MD25","MD24","MD23",@
"MD22","MD21","MD20","MD19","MD18","MD17","MD16","MD15","MD14","MD13","MD12",@
"MD11","MD10","MD9","MD8","MD7","MD6","MD5","MD4","MD3","MD2","MD1","MD0"

DIM SCTL(5)="WEIN","CSE","CSS","CSS2","OE"

;@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@
;@          TESTS BEGIN HERE              @
;@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@

;-----CONTINUITY TEST-----

SET DISPLAY "CONTACT..."
VS3=0.0V
ISVM MDC=-1MA,M(8V),2V,-2V
LIMIT MDC=1.5V,-1.5V
MEAS MDC(DEVPINS)
IF FAIL THEN ENTRY
        TNUM=0
        TSYM="CONT"
        MINLIM=-1.5V
        MAXLIM=1.5V
        READ FPIN TO PN, XPINS
        DO CONT1 I=1,PN
;               WRITE "CONTINUITY FAILS PIN ", XPINS(I) /
                SUSP(XPINS(I))=1
                TCOND=ASCII(XPINS(I),1,2)
                MEAS MDC(P(XPINS(I))):RESULT
                GOSUB OUTPUT
        CONT1:
```

```
        GOTO CONTINUE

EXIT
SET DISPLAY "           "

;*********************************
;       PREPARE DFM & AFM       *
;*********************************

RESET DFM ALL
DFM MODE=FAIL
DFM FCNT=2000
RESET AFM ALL
AFM RATE=HS
;       AFM Channels are Pn
;       SRAM4-1 MSB -> LSB
AFM CHANNEL=27,29,31,33,35,37,51,49@
            66,68,70,72,74,76,89,87@
            28,30,32,34,36,38,50,48@
            67,69,71,73,75,77,88,86

AFM ACTION=FT>FMX
;       AFM Addresses are LSB->MSB
AFM ADDRESS=X0-7,Y0-8

;*********************************
;       SRAM TEST               *
;*********************************

TNUM=1

TSYM="FUNC"
MINLIM=0.0
MAXLIM=0.0

SET DISPLAY TSYM

VS3=5.0V        ; VDD
VS1=5.0V        ; VPP

SELECT VTCONTROL ENABLE
SELECT LPAT INHIBIT     ; Let the pattern run to the end

TIME1=100MS:VS3
TIME2=100MS:OTHERS

RATE=1US,26US,7US,50NS
ACLK1=0NS:3,0NS
BCLK1=0.45US:3,20NS
CCLK1=0.5US:3,25NS
STRB1=0.95US:3,45NS
DREL1=0NS:3,0NS
DRET1=1US:3,50NS

IN1=5.0V,0.0V
IN2=2.0V,0.8V
OUT1=2.0V,0.8V
VT1=1.4V
IL1=-1MA,1MA
```

```
XABUS=IN1,NRZA,ACLK1,<X7-0>
YABUS=IN1,NRZA,ACLK1,<Y8-0>
MPERBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXH>
MDBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
U1BUS=IN1,NRZA,ACLK1,OUT1,STRB1,IL1,VT1,DRENRZ,DRE1,<D0-7>
CTLPINS=IN1,NRZA,ACLK1
WEIN=IN1,/RZZ,BCLK1,CCLK1

TCOND="SRAM1"
TEST TNUM
MEAS LPAT FUNC
IF PASS THEN RESULT=1.0
        ELSE RESULT=0.0

GOSUB OUTPUT
TNUM=TNUM+1

READ DFM FCNT TO FCOUNT
IF FCOUNT > 0 THEN ENTRY
        GOSUB DIAGSA
EXIT

RESET AFM MEMORY
RESET DFM MEMORY

TCOND="SRAM2"
MDBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
U2BUS=IN1,NRZA,ACLK1,OUT1,STRB1,IL1,VT1,DRENRZ,DRE1,<D0-7>

TEST TNUM
MEAS LPAT FUNC
IF PASS THEN RESULT=1.0
        ELSE RESULT=0.0

GOSUB OUTPUT
TNUM=TNUM+1

READ DFM FCNT TO FCOUNT
IF FCOUNT > 0 THEN ENTRY
        GOSUB DIAGSA
EXIT

RESET AFM MEMORY
RESET DFM MEMORY

TCOND="SRAM3"
MDBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
U3BUS=IN1,NRZA,ACLK1,OUT1,STRB1,IL1,VT1,DRENRZ,DRE1,<D0-7>

TEST TNUM
MEAS LPAT FUNC
IF PASS THEN RESULT=1.0
        ELSE RESULT=0.0

GOSUB OUTPUT
TNUM=TNUM+1

READ DFM FCNT TO FCOUNT
IF FCOUNT > 0 THEN ENTRY
        GOSUB DIAGSA
```

```
EXIT

RESET AFM MEMORY
RESET DFM MEMORY

TCOND="SRAM4"
MDBUS=IN1,NRZA,ACLK1,OUT1,STRB1,IL1,VT1,DRENRZ,DRE1,<FIXL>
MDBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
U4BUS=IN1,NRZA,ACLK1,OUT1,STRB1,IL1,VT1,DRENRZ,DRE1,<D0-7>

TEST TNUM
MEAS LPAT FUNC
IF PASS THEN RESULT=1.0
        ELSE RESULT=0.0

GOSUB OUTPUT
TNUM=TNUM+1

READ DFM FCNT TO FCOUNT
IF FCOUNT > 0 THEN ENTRY
        GOSUB DIAGSA
EXIT

RESET AFM MEMORY
RESET DFM MEMORY

;       SRAM7-5 MSB -> LSB
AFM CHANNEL=15,55,18,58,21,61,24,64,@
            54,17,57,20,60,23,63,26,@
            16,56,19,59,22,62,25,65

TCOND="SRAM5"
MDBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
MPERBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXH>
U5BUS=IN1,NRZA,ACLK1,OUT1,STRB1,IL1,VT1,DRENRZ,DRE1,<D0-7>

TEST TNUM
MEAS LPAT FUNC
IF PASS THEN RESULT=1.0
        ELSE RESULT=0.0

GOSUB OUTPUT
TNUM=TNUM+1

READ DFM FCNT TO FCOUNT
IF FCOUNT > 0 THEN ENTRY
        GOSUB DIAGSB
EXIT

RESET AFM MEMORY
RESET DFM MEMORY

TCOND="SRAM6"
MPERBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXH>
U6BUS=IN1,NRZA,ACLK1,OUT1,STRB1,IL1,VT1,DRENRZ,DRE1,<D0-7>

TEST TNUM
MEAS LPAT FUNC
IF PASS THEN RESULT=1.0
        ELSE RESULT=0.0
```

```
GOSUB OUTPUT
TNUM=TNUM+1

READ DFM FCNT TO FCOUNT
IF FCOUNT > 0 THEN ENTRY
        GOSUB DIAGSB
EXIT

RESET AFM MEMORY
RESET DFM MEMORY

TCOND="SRAM7"
MPERBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXH>
U7BUS=IN1,NRZA,ACLK1,OUT1,STRB1,IL1,VT1,DRENRZ,DRE1,<D0-7>

TEST TNUM
MEAS LPAT FUNC
IF PASS THEN RESULT=1.0
        ELSE RESULT=0.0

GOSUB OUTPUT
TNUM=TNUM+1

READ DFM FCNT TO FCOUNT
IF FCOUNT > 0 THEN ENTRY
        GOSUB DIAGSB
EXIT

;************************
;       ERASE           *
;************************

TSYM="ERASE"
TCOND="EPROMS"

VS1=12.0V
STRB4=0.95US:3

XABUS=IN1,NRZA,ACLK1,<FIXL>
YABUS=IN1,NRZA,ACLK1,<FIXL>
MPERBUS=IN1,NRZA,ACLK1,OUT1,STRB1,IL1,VT1,DRENRZ,DRE1,<FIXL>
MDBUS=IN1,NRZA,ACLK1,OUT1,STRB1,IL1,VT1,DRENRZ,DRE1,<FIXL>
CTLPINS=IN1,NRZA,ACLK1
WEIN=IN1,/RZZ,BCLK1,CCLK1
POLPINS=IN1,NRZA,ACLK1,OUT1,STRB4,IL1,VT1,DRENRZ,DRE1,MATCH,<FIXL>

TEST TNUM
MEAS LPAT ERASE
IF PASS THEN RESULT=1.0
        ELSE RESULT=0.0

GOSUB OUTPUT
TNUM=TNUM+1

TSYM="VERIFY"
TCOND="EPROM1"

VS1=5.0V
```

```
XABUS=IN1,NRZA,ACLK1,<X7-0>
YABUS=IN1,NRZA,ACLK1,<Y8-0>
MPERBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
MDBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
U1BUS=IN1,NRZA,ACLK1,OUT1,STRB1,IL1,VT1,DRENRZ,DRE1,<D0-7>
CTLPINS=IN1,NRZA,ACLK1
WEIN=IN1,/RZZ,BCLK1,CCLK1

TEST TNUM
MEAS LPAT VERIFY
IF PASS THEN RESULT=1.0
        ELSE RESULT=0.0

GOSUB OUTPUT
TNUM=TNUM+1

TCOND="EPROM2"
MPERBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
MDBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
U2BUS=IN1,NRZA,ACLK1,OUT1,STRB1,IL1,VT1,DRENRZ,DRE1,<D0-7>
TEST TNUM
MEAS LPAT VERIFY
IF PASS THEN RESULT=1.0
        ELSE RESULT=0.0

GOSUB OUTPUT
TNUM=TNUM+1

TCOND="EPROM3"
MPERBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
MDBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
U3BUS=IN1,NRZA,ACLK1,OUT1,STRB1,IL1,VT1,DRENRZ,DRE1,<D0-7>
TEST TNUM
MEAS LPAT VERIFY
IF PASS THEN RESULT=1.0
        ELSE RESULT=0.0

GOSUB OUTPUT
TNUM=TNUM+1

TCOND="EPROM4"
MPERBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
MDBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
U4BUS=IN1,NRZA,ACLK1,OUT1,STRB1,IL1,VT1,DRENRZ,DRE1,<D0-7>
TEST TNUM
MEAS LPAT VERIFY
IF PASS THEN RESULT=1.0
        ELSE RESULT=0.0

GOSUB OUTPUT
TNUM=TNUM+1

TCOND="EPROM5"
MPERBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
MDBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
U5BUS=IN1,NRZA,ACLK1,OUT1,STRB1,IL1,VT1,DRENRZ,DRE1,<D0-7>
TEST TNUM
MEAS LPAT VERIFY
IF PASS THEN RESULT=1.0
        ELSE RESULT=0.0
```

```
GOSUB OUTPUT
TNUM=TNUM+1

TCOND="EPROM6"
MPERBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
MDBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
U6BUS=IN1,NRZA,ACLK1,OUT1,STRB1,IL1,VT1,DRENRZ,DRE1,<D0-7>
TEST TNUM
MEAS LPAT VERIFY
IF PASS THEN RESULT=1.0
        ELSE RESULT=0.0

GOSUB OUTPUT
TNUM=TNUM+1

TCOND="EPROM7"
MPERBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
MDBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
U7BUS=IN1,NRZA,ACLK1,OUT1,STRB1,IL1,VT1,DRENRZ,DRE1,<D0-7>
TEST TNUM
MEAS LPAT VERIFY
IF PASS THEN RESULT=1.0
        ELSE RESULT=0.0

GOSUB OUTPUT
TNUM=TNUM+1

;****************************************
;*       WRITE EPROM TRUE DATA          *
;****************************************

TSYM="WRNEW"
TCOND="EPROM5"
GOSUB DFMAFM    ; SETUP THE DFM & AFM TO CATCH ERRORS

VS1=12.0V

XABUS=IN1,NRZA,ACLK1,<X7-0>
YABUS=IN1,NRZA,ACLK1,<Y8-0>
MPERBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
MDBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
U1BUS=IN1,NRZA,ACLK1,OUT1,STRB4,IL1,VT1,DRENRZ,DRE1,MATCH,<D0-7>
U2BUS=IN1,NRZA,ACLK1,OUT1,STRB4,IL1,VT1,DRENRZ,DRE1,MATCH,<D0-7>
U3BUS=IN1,NRZA,ACLK1,OUT1,STRB4,IL1,VT1,DRENRZ,DRE1,MATCH,<D0-7>
U4BUS=IN1,NRZA,ACLK1,OUT1,STRB4,IL1,VT1,DRENRZ,DRE1,MATCH,<D0-7>
U5BUS=IN1,NRZA,ACLK1,OUT1,STRB4,IL1,VT1,DRENRZ,DRE1,MATCH,<D0-7>
U6BUS=IN1,NRZA,ACLK1,OUT1,STRB4,IL1,VT1,DRENRZ,DRE1,MATCH,<D0-7>
U7BUS=IN1,NRZA,ACLK1,OUT1,STRB4,IL1,VT1,DRENRZ,DRE1,MATCH,<D0-7>
CTLPINS=IN1,NRZA,ACLK1
WEIN=IN1,/RZZ,BCLK1,CCLK1

TEST TNUM
SELECT LPAT MATCH INHIBIT
MEAS LPAT WRNEW
IF PASS THEN RESULT=1.0
        ELSE RESULT=0.0

GOSUB OUTPUT
TNUM=TNUM+1
```

```
IF RESULT = 0.0 THEN ENTRY
        GOSUB DIAGEW
EXIT

;*********************************
;*       READ TRUE DATA          *
;*********************************

RESET AFM MEMORY
RESET DFM MEMORY
DFM MODE FAIL
DFM FCNT=2000

XABUS=IN1,NRZA,ACLK1,<X7-0>
YABUS=IN1,NRZA,ACLK1,<Y8-0>
CTLPINS=IN1,NRZA,ACLK1
WEIN=IN1,/RZZ,BCLK1,CCLK1

TSYM="RDNEW"
VS1=5.0V

TCOND="EP4-1"
MPERBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
MDBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
U1BUS=IN1,NRZA,ACLK1,OUT1,STRB4,IL1,VT1,DRENRZ,DRE1,MATCH,<D0-7>
U2BUS=IN1,NRZA,ACLK1,OUT1,STRB4,IL1,VT1,DRENRZ,DRE1,MATCH,<D0-7>
U3BUS=IN1,NRZA,ACLK1,OUT1,STRB4,IL1,VT1,DRENRZ,DRE1,MATCH,<D0-7>
U4BUS=IN1,NRZA,ACLK1,OUT1,STRB4,IL1,VT1,DRENRZ,DRE1,MATCH,<D0-7>
SELECT LPAT INHIBIT
TEST TNUM
WAIT TIME 150MS
MEAS LPAT RDNEW
IF PASS THEN RESULT=1.0
        ELSE RESULT=0.0
GOSUB OUTPUT
TNUM=TNUM+1

READ DFM FCNT TO FCOUNT
IF FCOUNT > 0 THEN ENTRY
        GOSUB DIAGEA
EXIT

RESET AFM MEMORY
RESET DFM MEMORY

;       EPROM7-5 MSB -> LSB
AFM CHANNEL=15,55,18,58,21,61,24,64,@
            54,17,57,20,60,23,63,26,@
            16,56,19,59,22,62,25,65

TCOND="EP7-5"
MPERBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
MDBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
U5BUS=IN1,NRZA,ACLK1,OUT1,STRB4,IL1,VT1,DRENRZ,DRE1,MATCH,<D0-7>
U6BUS=IN1,NRZA,ACLK1,OUT1,STRB4,IL1,VT1,DRENRZ,DRE1,MATCH,<D0-7>
U7BUS=IN1,NRZA,ACLK1,OUT1,STRB4,IL1,VT1,DRENRZ,DRE1,MATCH,<D0-7>
TEST TNUM
WAIT TIME 150MS
MEAS LPAT RDNEW
```

```
SELECT LPAT NORMAL
IF PASS THEN RESULT=1.0
        ELSE RESULT=0.0
GOSUB OUTPUT
TNUM=TNUM+1

READ DFM FCNT TO FCOUNT
IF FCOUNT > 0 THEN ENTRY
       GOSUB DIAGEB
EXIT

RESET AFM MEMORY
RESET DFM MEMORY

;*********************************
;*       ERASE                   *
;*********************************

TSYM="ERASE2"
TCOND="EPROMS"

VS1=12.0V

XABUS=IN1,NRZA,ACLK1,<FIXL>
YABUS=IN1,NRZA,ACLK1,<FIXL>
MPERBUS=IN1,NRZA,ACLK1,OUT1,STRB1,IL1,VT1,DRENRZ,DRE1,<FIXL>
MDBUS=IN1,NRZA,ACLK1,OUT1,STRB1,IL1,VT1,DRENRZ,DRE1,<FIXL>
CTLPINS=IN1,NRZA,ACLK1
WEIN=IN1,/RZZ,BCLK1,CCLK1
POLPINS=IN1,NRZA,ACLK1,OUT1,STRB4,IL1,VT1,DRENRZ,DRE1,MATCH,<FIXL>

TEST TNUM
MEAS LPAT ERASE
IF PASS THEN RESULT=1.0
        ELSE RESULT=0.0

GOSUB OUTPUT
TNUM=TNUM+1

;*****************************************
;*       WRITE INVERSE CHECKERBOARD      *
;*****************************************

TSYM="WRNEWI"
TCOND="EPROMS"
GOSUB DFMAFM     ; SETUP THE DFM & AFM TO CATCH ERRORS

VS1=12.0V

XABUS=IN1,NRZA,ACLK1,<X7-0>
YABUS=IN1,NRZA,ACLK1,<Y8-0>
MPERBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
MDBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
U1BUS=IN1,NRZA,ACLK1,OUT1,STRB4,IL1,VT1,DRENRZ,DRE1,MATCH,<D0-7>
U2BUS=IN1,NRZA,ACLK1,OUT1,STRB4,IL1,VT1,DRENRZ,DRE1,MATCH,<D0-7>
U3BUS=IN1,NRZA,ACLK1,OUT1,STRB4,IL1,VT1,DRENRZ,DRE1,MATCH,<D0-7>
U4BUS=IN1,NRZA,ACLK1,OUT1,STRB4,IL1,VT1,DRENRZ,DRE1,MATCH,<D0-7>
U5BUS=IN1,NRZA,ACLK1,OUT1,STRB4,IL1,VT1,DRENRZ,DRE1,MATCH,<D0-7>
U6BUS=IN1,NRZA,ACLK1,OUT1,STRB4,IL1,VT1,DRENRZ,DRE1,MATCH,<D0-7>
U7BUS=IN1,NRZA,ACLK1,OUT1,STRB4,IL1,VT1,DRENRZ,DRE1,MATCH,<D0-7>
```

```
CTLPINS=IN1,NRZA,ACLK1
WEIN=IN1,/RZZ,BCLK1,CCLK1

TEST TNUM
SELECT LPAT MATCH INHIBIT
MEAS LPAT WRNEWI
IF PASS THEN RESULT=1.0
        ELSE RESULT=0.0
GOSUB OUTPUT
TNUM=TNUM+1

IF RESULT = 0.0 THEN ENTRY
        GOSUB DIAGEW
EXIT

;*****************************************
;*       READ INVERSE CHECKERBOARD       *
;*****************************************

;*****************************************
;*       READ INVERSE DATA               *
;*****************************************

RESET AFM MEMORY
RESET DFM MEMORY
DFM MODE FAIL
DFM FCNT=2000

XABUS=IN1,NRZA,ACLK1,<X7-0>
YABUS=IN1,NRZA,ACLK1,<Y8-0>
CTLPINS=IN1,NRZA,ACLK1
WEIN=IN1,/RZZ,BCLK1,CCLK1

TSYM="RDNEWI"
VS1=5.0V

TCOND="EP4-1"
MPERBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
MDBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
U1BUS=IN1,NRZA,ACLK1,OUT1,STRB4,IL1,VT1,DRENRZ,DRE1,MATCH,<D0-7>
U2BUS=IN1,NRZA,ACLK1,OUT1,STRB4,IL1,VT1,DRENRZ,DRE1,MATCH,<D0-7>
U3BUS=IN1,NRZA,ACLK1,OUT1,STRB4,IL1,VT1,DRENRZ,DRE1,MATCH,<D0-7>
U4BUS=IN1,NRZA,ACLK1,OUT1,STRB4,IL1,VT1,DRENRZ,DRE1,MATCH,<D0-7>
SELECT LPAT INHIBIT
TEST TNUM
WAIT TIME 150MS
MEAS LPAT RDNEWI
IF PASS THEN RESULT=1.0
        ELSE RESULT=0.0
GOSUB OUTPUT
TNUM=TNUM+1

READ DFM FCNT TO FCOUNT
IF FCOUNT > 0 THEN ENTRY
        GOSUB DIAGEA
EXIT

RESET AFM MEMORY
RESET DFM MEMORY
```

```
;       EPROM7-5 MSB -> LSB
AFM CHANNEL=15,55,18,58,21,61,24,64,@
            54,17,57,20,60,23,63,26,@
            16,56,19,59,22,62,25,65

TCOND="EP7-5"
MPERBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
MDBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
U5BUS=IN1,NRZA,ACLK1,OUT1,STRB4,IL1,VT1,DRENRZ,DRE1,MATCH,<D0-7>
U6BUS=IN1,NRZA,ACLK1,OUT1,STRB4,IL1,VT1,DRENRZ,DRE1,MATCH,<D0-7>
U7BUS=IN1,NRZA,ACLK1,OUT1,STRB4,IL1,VT1,DRENRZ,DRE1,MATCH,<D0-7>
TEST TNUM
WAIT TIME 150MS
MEAS LPAT RDNEWI
SELECT LPAT NORMAL
IF PASS THEN RESULT=1.0
        ELSE RESULT=0.0
GOSUB OUTPUT
TNUM=TNUM+1

READ DFM FCNT TO FCOUNT
IF FCOUNT > 0 THEN ENTRY
        GOSUB DIAGEB
EXIT

RESET AFM MEMORY
RESET DFM MEMORY

;*********************************
;*       ERASE                   *
;*********************************

TSYM="ERASE3"
TCOND="EPROMS"

VS1=12.0V

XABUS=IN1,NRZA,ACLK1,<FIXL>
YABUS=IN1,NRZA,ACLK1,<FIXL>
MPERBUS=IN1,NRZA,ACLK1,OUT1,STRB1,IL1,VT1,DRENRZ,DRE1,<FIXL>
MDBUS=IN1,NRZA,ACLK1,OUT1,STRB1,IL1,VT1,DRENRZ,DRE1,<FIXL>
CTLPINS=IN1,NRZA,ACLK1
WEIN=IN1,/RZZ,BCLK1,CCLK1
POLPINS=IN1,NRZA,ACLK1,OUT1,STRB4,IL1,VT1,DRENRZ,DRE1,MATCH,<FIXL>

TEST TNUM
MEAS LPAT ERASE
IF PASS THEN RESULT=1.0
        ELSE RESULT=0.0

GOSUB OUTPUT
TNUM=TNUM+1

TSYM="VERIFY2"
TCOND="EPROM1"

VS1=5.0V

XABUS=IN1,NRZA,ACLK1,<X7-0>
YABUS=IN1,NRZA,ACLK1,<Y8-0>
```

```
MPERBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
MDBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
U1BUS=IN1,NRZA,ACLK1,OUT1,STRB1,IL1,VT1,DRENRZ,DRE1,<D0-7>
CTLPINS=IN1,NRZA,ACLK1
WEIN=IN1,/RZZ,BCLK1,CCLK1

TEST TNUM
MEAS LPAT VERIFY
IF PASS THEN RESULT=1.0
        ELSE RESULT=0.0

GOSUB OUTPUT
TNUM=TNUM+1

TCOND="EPROM2"
MPERBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
MDBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
U2BUS=IN1,NRZA,ACLK1,OUT1,STRB1,IL1,VT1,DRENRZ,DRE1,<D0-7>
TEST TNUM
MEAS LPAT VERIFY
IF PASS THEN RESULT=1.0
        ELSE RESULT=0.0

GOSUB OUTPUT
TNUM=TNUM+1

TCOND="EPROM3"
MPERBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
MDBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
U3BUS=IN1,NRZA,ACLK1,OUT1,STRB1,IL1,VT1,DRENRZ,DRE1,<D0-7>
TEST TNUM
MEAS LPAT VERIFY
IF PASS THEN RESULT=1.0
        ELSE RESULT=0.0

GOSUB OUTPUT
TNUM=TNUM+1

TCOND="EPROM4"
MPERBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
MDBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
U4BUS=IN1,NRZA,ACLK1,OUT1,STRB1,IL1,VT1,DRENRZ,DRE1,<D0-7>
TEST TNUM
MEAS LPAT VERIFY
IF PASS THEN RESULT=1.0
        ELSE RESULT=0.0

GOSUB OUTPUT
TNUM=TNUM+1

TCOND="EPROM5"
MPERBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
MDBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
U5BUS=IN1,NRZA,ACLK1,OUT1,STRB1,IL1,VT1,DRENRZ,DRE1,<D0-7>
TEST TNUM
MEAS LPAT VERIFY
IF PASS THEN RESULT=1.0
        ELSE RESULT=0.0

GOSUB OUTPUT
```

```
TNUM=TNUM+1

TCOND="EPROM6"
MPERBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
MDBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
U6BUS=IN1,NRZA,ACLK1,OUT1,STRB1,IL1,VT1,DRENRZ,DRE1,<D0-7>
TEST TNUM
MEAS LPAT VERIFY
IF PASS THEN RESULT=1.0
        ELSE RESULT=0.0

GOSUB OUTPUT
TNUM=TNUM+1

TCOND="EPROM7"
MPERBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
MDBUS=IN1,NRZA,ACLK1,OUT1,IL1,VT1,DRENRZ,DRE1,<FIXL>
U7BUS=IN1,NRZA,ACLK1,OUT1,STRB1,IL1,VT1,DRENRZ,DRE1,<D0-7>
TEST TNUM
MEAS LPAT VERIFY
IF PASS THEN RESULT=1.0
        ELSE RESULT=0.0

GOSUB OUTPUT
TNUM=TNUM+1


GOTO CONTINUE

;#############################################################################
;
;       WRITE TEST RESULT ROUTINE
;
;#############################################################################
OUTPUT:

TCOND=ASCII(TCOND,2,8)
TSYM=ASCII(TSYM,2,8)
LIMCOND=0                               ;INITIALIZE FOR BOTH MAX & MIN LIMITS
PF="PASS    "                           ;ASSUME INNOCENT UNTIL PROVEN GUILTY
OMIN=MINLIM                             ;INITIALIZE MIN LIMIT OUTPUT VARIABLE
OMAX=MAXLIM                             ;INITIALIZE MAX LIMIT OUTPUT VARIABLE

MINTYP=CODE(MINLIM)
MAXTYP=CODE(MAXLIM)

IF MINTYP=2 AND MAXTYP<>2 THEN LIMCOND=1;NO MINIMUM LIMIT
IF MAXTYP=2 AND MINTYP<>2 THEN LIMCOND=2;NO MAXIMUM LIMIT
IF MAXTYP=2 AND MINTYP=2 THEN LIMCOND=3 ;NEITHER MAX LIMIT OR MIN LIMIT

IF LIMCOND=0 THEN ENTRY                 ;JUDGE BOTH LIMITS
        IF RESULT<MINLIM OR RESULT>MAXLIM THEN PF="FAIL ***"
        EXIT

IF LIMCOND=1 THEN ENTRY                 ;JUDGE ONLY MAXIMUM LIMIT
        OMIN="NONE      "
        IF RESULT>MAXLIM THEN PF="FAIL ***"
        EXIT

IF LIMCOND=2 THEN ENTRY                 ;JUDGE ONLY MINIMUM LIMIT
```

```
        OMAX="NONE      "
        IF RESULT<MINLIM THEN PF="FAIL ***"
        EXIT

IF LIMCOND=3 THEN ENTRY                 ;TEST IS FUNCTIONAL, NO JUDGE LIMITS
        OMAX="NONE      "
        OMIN="NONE      "
        IF RESULT<0.5 THEN PF="FAIL ***"
        EXIT

IF PF(1,1)="F" THEN ENTRY
                FCNT=FCNT+1       ; GET TRACK OF THE TOTAL NUMBER OF
                ;SET SOUND 6        ; FAILURES
                ;WAIT TIME 500MS
                ;RESET SOUND
                EXIT

IF FK=.1 THEN ENTRY
        WRITE [1,2(6,0)] TNUM,"   "
        WRITE [1,4(8,0)] TSYM,"   "
        WRITE [1,4(8,0)] TCOND,"   "
        WRITE [1,2(11,3)] OMAX,"   "
        WRITE [1,2(11,3)] OMIN,"   "
        RCODE=CODE(RESULT)
        IF RCODE=2 THEN WRITE [1,2(8,3)] RESULT,"      "
                   ELSE WRITE [1,2(11,3)] RESULT,"   "
        WRITE [1,2(9,3)] PF,/
EXIT

GOTO CONTINUE

;#############################################################################
;
;       WRITE FOOTER ROUTINE
;
;#############################################################################
DOFOOT:

; INDICATE FAILURE SUSPECTS

DO FOOT1 I=1,92
        IF SUSP(I)=1 THEN ENTRY
                WRITE [1] "POSSIBLE PROBLEM WITH PIN ", I /
        EXIT
FOOT1:

READ CNT99 TO SERNUM
IF FCNT=0 THEN ENTRY
  WRITE [1] / "SERIAL NUMBER ",SERNUM,"PASSES" /
  RESET RESULT 3
EXIT
ELSE ENTRY
  WRITE [1] / "SERIAL NUMBER ",SERNUM,"** FAILS **" /
  SET RESULT 3
EXIT

GOTO CONTINUE
;#############################################################################
;
;       WRITE HEADER ROUTINE
```

```
;
;###############################################################################
DOHEAD:

STRING XTIME(17)

IF FK=.1 THEN ENTRY
  WRITE ?<14>?

  WRITE [1] "DATASET:      " DATASET /
  WRITE [1] "PART NUMBER:  " PRTNMBR /
  XTIME=GDAY(1)
  WRITE [1] "DATE:         " XTIME /
  READ CNT99 TO SERNUM
  WRITE [1] "SERIAL NO.:   " SERNUM //

  WRITE [1] " TEST      SYM       COND      MAXIMUM       MINIMUM       RESULT
  WRITE [1] "------  ---------  -------  -----------  -----------  -----------
EXIT

; CLEAR THE ARRAY OF SUSPECT PINS

DO HEAD1 I=1,92
        SUSP(I)=0
HEAD1:

GOTO CONTINUE


;###############################################################################
;
;       INITIALIZATION ROUTINE
;
;###############################################################################
DOINIT:

RESET DISPLAY
WRITE [1] ?<14>?

WRITE [1] // "DATASET:        " DATASET /
WRITE [1]    "PART NUMBER:    " PRTNMBR /
WRITE [1]    "AUTHOR:         " PRGMER /
WRITE [1]    "RELEASE DATE:   " RELDATE /
WRITE [1]    "REQUIREMENTS:   " REQS /
WRITE [1,5(4)]    "LOAD BOARD:     " BRDID //

WRITE [1] "NOTE: DATA LOGGING IS CONTROLLED BY FUNCTION KEY #1.  DATA LOG" /
WRITE [1] "      DESTINATION IS SET USING THE 'S' CONTROLLER COMMAND." //

INIT1:
WRITE [1]      "PRESS <S> TO STOP",/
INPUT [1,4(0)] "       <C> TO CONTINUE ",C,/
IF C="S" THEN STOP
         ELSE IF C<>"C" THEN GOTO INIT1

READ PBID TO I
IF I<>BRDID THEN ENTRY
        WRITE [1] / "WRONG PERFORMANCE BOARD!" /
        WRITE [1,5(4)]   "BOARD ID NUMBER:  " I /
        WRITE [1,5(4)]   "SHOULD BE:  " BRDID //
```

```
        STOP
        EXIT

GO TO CONTINUE

;#############################################################################
;
;       SRAM DIAGNOSTIC ROUTINE (FOR SRAM1-4)
;
;#############################################################################
DIAGSA:
        GOSUB DIAGM

        READ FUNC1(EP4321) TO FNDATA
        WRITE [1,5],"FUNC1(SR4321) ",FNDATA,/
GO TO CONTINUE

;#############################################################################
;
;       SRAM DIAGNOSTIC ROUTINE (FOR SRAM5-7)
;
;#############################################################################
DIAGSB:
        GOSUB DIAGM

        READ FUNC1(EP765) TO FNDATA
        WRITE [1,5],"FUNC1(SR765) ",FNDATA,/
GO TO CONTINUE

;#############################################################################
;
;       EPROM DIAGNOSTIC ROUTINE (FOR EPROM1-4)
;
;#############################################################################
DIAGEA:
        GOSUB DIAGM

        READ FUNC1(EP4321) TO FNDATA
        WRITE [1,5],"FUNC1(EP4321) ",FNDATA,/
GOTO CONTINUE

;#############################################################################
;
;       EPROM DIAGNOSTIC ROUTINE (FOR EPROM5-7)
;
;#############################################################################
DIAGEB:
        GOSUB DIAGM

        READ FUNC1(EP765) TO FNDATA
        WRITE [1,5],"FUNC1(EP765) ",FNDATA,/
GOTO CONTINUE

;#############################################################################
;
;       SUBROUTINE TO READ & DISPLAY DFM / AFM MEMORY
;
;#############################################################################
DIAGM:
        WRITE [1,5],"FCNT= ",FCOUNT,/
```

```
        READ DFM PCNT TO PCOUNT
        WRITE [1,5],"PCNT= ",PCOUNT,/

        READ DFM STATUS TO STATUS
        WRITE [1,5],"STATUS= ",STATUS,/

        READ DFM DFMA TO DFMADD
        WRITE [1,5],"DFMA= ",DFMADD,/

        DO RDX I=0,19
                READ DFM X(I) TO DFMX
                READ DFM Y(I) TO DFMY
                FADDR = (DFMY*#100)+DFMX
                READ AFM FT(FADDR) TO AFMMEM
                WRITE [1,5],"FADDR: ",FADDR," AFMMEM: ",AFMMEM

                FHIGH = SR(FADDR,16)
                FMIDD = SR(FADDR,8)
                EXPDATA = (FHIGH+FMIDD+FADDR).AND.#FF
                INVDATA = (.NOT.EXPDATA).AND.#FF
                WRITE [1,5(2)] " EXPDATA: ",EXPDATA," INVDATA: ",INVDATA,/

        RDX:
GOTO CONTINUE

;#############################################################################
;
;       EPROM WRITE DIAGNOSTIC ROUTINE (FOR EPROM4-1)
;
;#############################################################################
DIAGEW:
        WRITE "DIAGNOSTIC OUTPUT FOR EPROMS 4-1 ONLY.",/
        READ DFM FCNT TO FCOUNT
        WRITE [1,5],"FCNT= ",FCOUNT,/

        READ DFM PCNT TO PCOUNT
        WRITE [1,5],"PCNT= ",PCOUNT,/

        READ DFM STATUS TO STATUS
        WRITE [1,5],"STATUS= ",STATUS,/

        READ DFM DFMA TO DFMADD
        WRITE [1,5],"DFMA= ",DFMADD,/
        LOOPER = MOD(DFMADD/2048)-1     ;COMPUTE LAST DFM ADDRESS WRITTEN

        DO RDTOF0 I=LOOPER-2,LOOPER
                READ DFM TOFL(I) TO TOFAIL
                READ DFM PFPC1(I) TO STEADD
                READ DFM TPD(I) TO DFMTPD
                WRITE [1,5],"TOFL",I," ",TOFAIL," PFPC1 ",STEADD," TPD ",DFMTPD,
        RDTOF0:

        DO RDXY0 I=LOOPER-2,LOOPER
                READ DFM Y(I) TO DFMY
                READ DFM X(I) TO DFMX
                WRITE [1,5],"ADDR",I," Y ",DFMY," X ",DFMX,/
        RDXY0:

        DO RDAFM0 I=0,1
```

```
                READ AFM FT(I) TO AFMMEM
                WRITE [1,5],"AFM",I,AFMMEM,/
        RDAFM0:

        READ FUNC1(EP4321) TO FNDATA
        WRITE [1,5],"FUNC1(EP4321) ",FNDATA,/
GOTO CONTINUE

;************************************************
;       PREPARE DFM & AFM (DEVICES 4-1 ONLY)    *
;************************************************
DFMAFM:
        RESET DFM ALL
        DFM MODE=ALL
        DFM FCNT=0          ; LET DFM RUN TO END
        RESET AFM ALL
        AFM RATE=HS
;       AFM Channels are Pn
;       EPROM4-1 MSB -> LSB
        AFM CHANNEL=27,29,31,33,35,37,51,49@
            66,68,70,72,74,76,89,87@
            28,30,32,34,36,38,50,48@
            67,69,71,73,75,77,88,86
        AFM ACTION=FT>FMX
;       AFM Addresses are LSB->MSB
        AFM ADDRESS=X0-7,Y0-8
GOTO CONTINUE

END
```

Test Article: PMM
Test Engineer: Grant Ericksson
Test Technician: Matthew Miller
Test Observer:

Date: 9/17/98
Page: 1 of 3

Test Setup Photographs:

Interference test on signal MOI3 (PMM pin 49)

1 GHz
+ 24.5 dbm CW - Pass
+ 27.5 dbm - Pass
+ 30.5 dbm - Pass
+ 31.5 dbm - Fail

1.2 GHz
+ 31.5 dbm - Pass
+ 32.5 dbm - Pass
+ 33.5 dbm - Fail

1.4 GHz
33.3 dbm - Fail
30.3 dbm - Fail
29.3 dbm - Fail
28.3 dbm - Pass

Test Part #
Test Sequence #

Test Article: PMM
Test Engineer: Grant Erickson
Test Technician:
Test Observer:

Date: 9/17/98
Page: 2 of 3

Test Setup Photographs:

Test Part #
Test Sequence #

Interference Test on MPER13
(Test Fixture Line 2)

1 GHz
+21.5 dbm CM – Pass
+22.5 dbm – Pass
+23.5 dbm – Pass
+24.5 dbm – Fail

1.2 GHz
+28.5 dbm – Fail
+25.5 dbm – Fail
+24.5 dbm – pass

1.4 GHz
+27.3 dbm – Fail
+26.3 dbm – Pass

1.5 GHz
+30.5 dbm – Pass
+31.5 dbm – Pass
+32.5 dbm – Fail

Test Article: PMM
Test Engineer: Grant Erickson
Test Technician: Matthew Miller
Test Observer:

Date: 9/17/98
Page: 3 of 3

Test Setup Photographs:

Test Part #
Test Sequence #

Interference Test on Signal MD 13 (PMM Pin 49) Continued

1.6 GHz
- 31.4 dbm - Pass
- 34.4 dbm - Pass
- 36.4 dbm - Pass
- 37.4 dbm - Fail

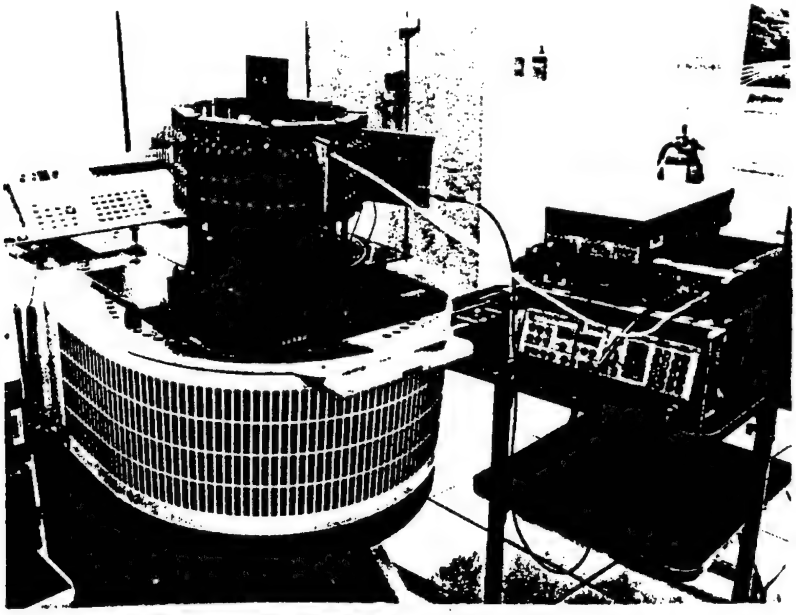
1.8 GHz
- 29.6 dbm - Pass
(could not induce failure)

2.0 GHz
- 31.1 dbm - Pass
(could not induce failure)

Test Article: PMM
Test Engineer: Grant Ericksen
Test Technician: Matthew Miller
Test Observer:

Date: 9/28/98
Page: 1 of 6

Test Setup Photographs:



Test Part #
Test Sequence #

Interference test on MPER 13
(test Fixture Line 2)

100 MHz
+17.3 dbm CW Pass
+18.3 fail

300 MHz
+17.3 dbm pass
+18.3 dbm fail

Test Article: PMM
Test Engineer: Grant Erickson
Test Technician:
Test Observer:

Date: 9/28/98
Page: 2 of 6

Test Setup Photographs:

Test Part #
Test Sequence #

MPER 13 interference test (cont.)

500 MHz
+16.8 dbm CW - Pass
+18.8 dbm - Pass
+19.8 dbm - Fail

600 MHz
+25.2 dbm - Pass
+26.2 dbm - Pass
+27.2 dbm - Fail

700 MHz
+21.4 dbm - Pass
+23.4 dbm - Pass
+24.4 dbm - Pass
+25.4 dbm - Fail

800 MHz
+15.8 dbm - Pass
+24.7 dbm - Pass
+25.7 dbm - Fail

Test Article: PMM
Test Engineer: Grant Ericksen
Test Technician:
Test Observer:

Date: 9/28/98
Page: 3 of 6

Test Setup Photographs:

Test Part #
Test Sequence #

MPERB Interference Test (Cont.)

900 MHz
+13.7 dbm - Pass
+23.7 dbm - Fail
+21.7 dbm - Pass
+22.7 dbm - Pass

1.0 GHz
+25.0 dbm - Pass
+26.0 dbm - Fail
+25.5 dbm - Pass
+26.5 dbm - Fail

1.2 GHz
+30.5 dbm - Fail
+27.5 dbm - Fail
+24.5 dbm - Fail
+23.5 dbm - Pass
+24.5 dbm - Pass
+25.5 dbm - Fail

Test Article: PMM
Test Engineer: Grant Erickson
Test Technician:
Test Observer:

Date: 9/28/98
Page: 4 of 6

Test Setup Photographs:

Test Part #
Test Sequence #

MPER 13 Interference test (cont)

1.4 GHz

+20.8 dbm	- Pass
+23.8	- Pass
+26.8	- Pass
+30.8	- Fail
+28.8	- Fail
+27.8 dbm	- Pass

1.6 GHz

+29.4 dbm	- Pass
+32.4	- Pass
+36.4	- Pass
+37.4	- Fail

1.8 GHz

+37.4 dbm	- Pass
+40.4 dbm	- Pass
+43.4	- Fail
+41.4	- Fail
+40.4	- Pass

EMEAP Susceptibility

Test Article: PMM
Test Engineer: Grant Erickson
Test Technician:
Test Observer:

Date: 9/28/98
Page: 5 of 6

Test Setup Photographs:

Test Part #
Test Sequence #

Interference Test on MPER13
(Tst Fixture Line 2) 2GHz
+30 dbm (1watt) Pass
+33dbm 2w Pass +36dbm Pass
+40dbm (10w) Pass

Interference Test on MPER13
(Test Fixture Line2) 3GHz
+30dBm (1watt) Pass
+33dBm (2watt) Pass
+36dBm (4watt) Pass
+39dBm (8watt) Pass
+40dBm (≈10W) Pass
+42dBm (16W) Pass

Test Fixture Line 2 3.5GHz
+30dBm (1W) Pass
+33dBm (2W) Pass
+36 dBm (4W) Pass
+39dBm (8W) Pass
+42dBm (16W)

EMEAP Susceptibility

Test Article: PMM
Test Engineer: Grant Erickson
Test Technician:
Test Observer:

Date: 9/28/98
Page: 6 of 6

Test Setup Photographs:

Test Part #
Test Sequence #

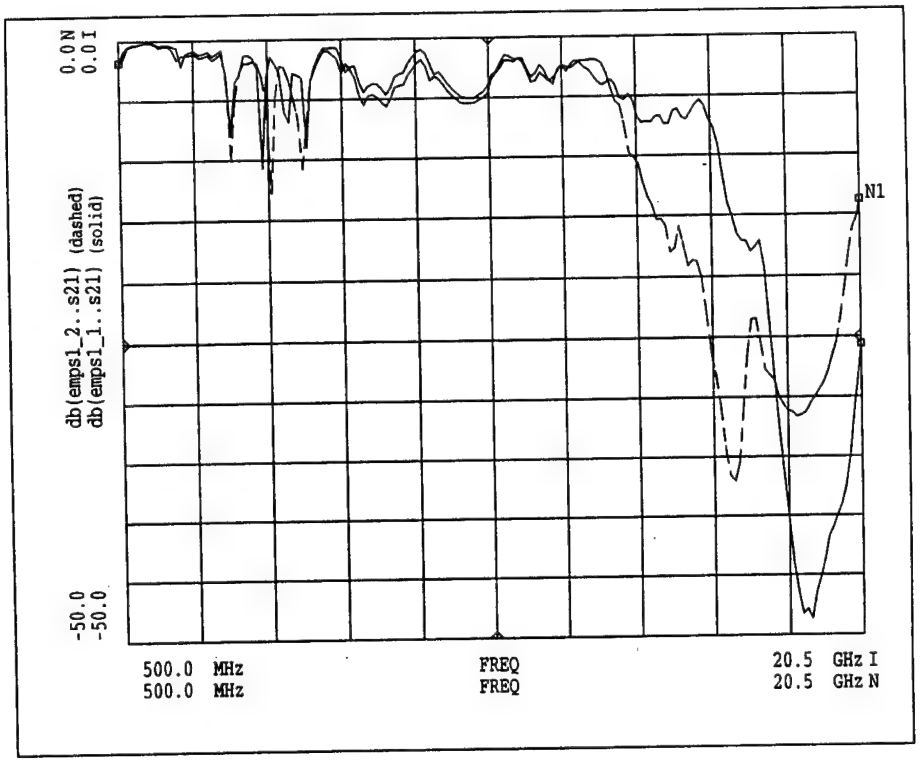
4.0 GHz
+30 dbm Pass
+37 dbm Pass
+40 dbm Pass
+42 dbm Pass

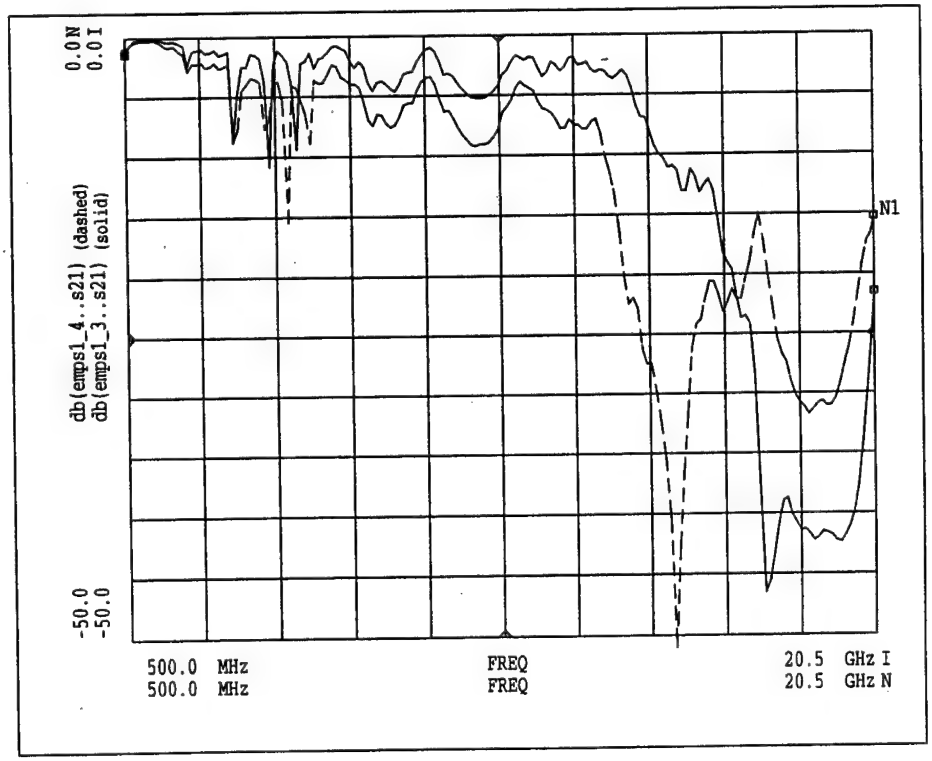
5.0 GHz
+30 dbm Pass
+40 dbm Pass

6.0 GHz
+30 dbm Pass
+40 dbm Pass

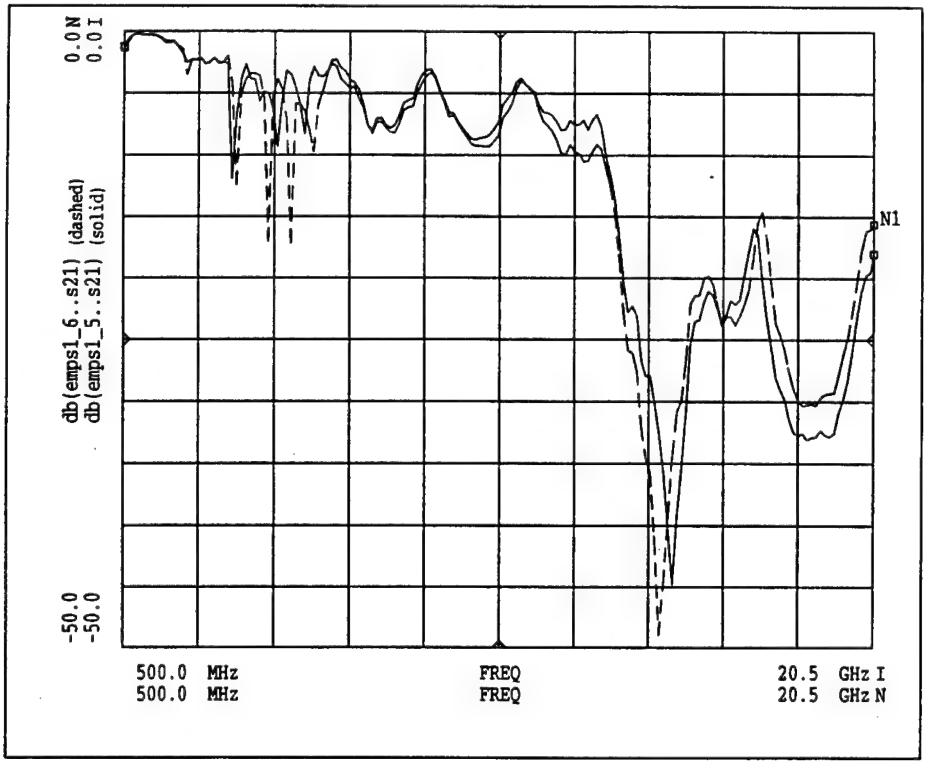
7.0 GHz
+30 dbm Pass
+40 dbm Pass

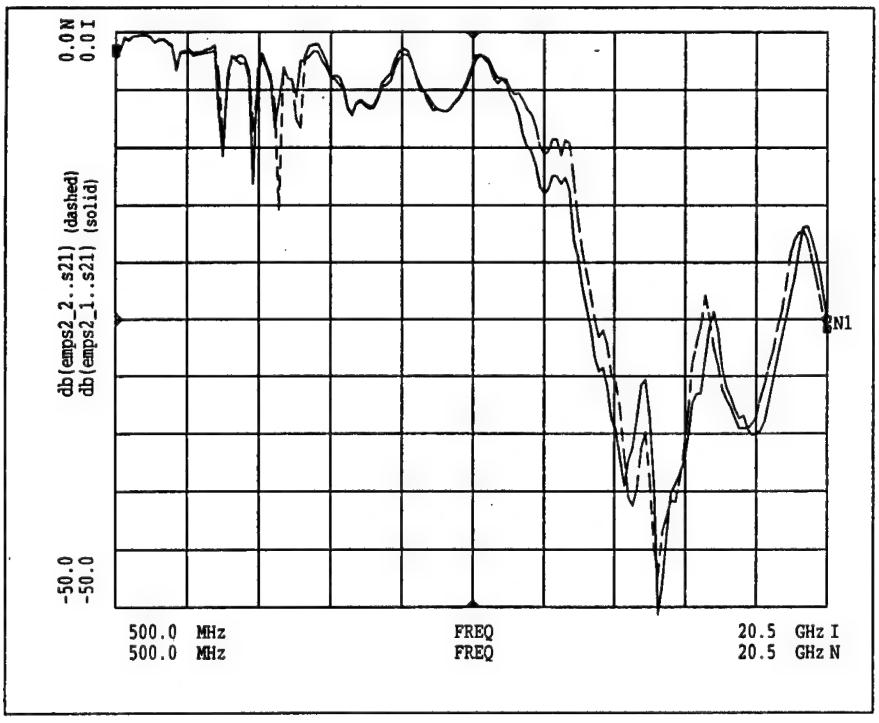
Appendix H –Diplexer Signal Combiner S21 Performance



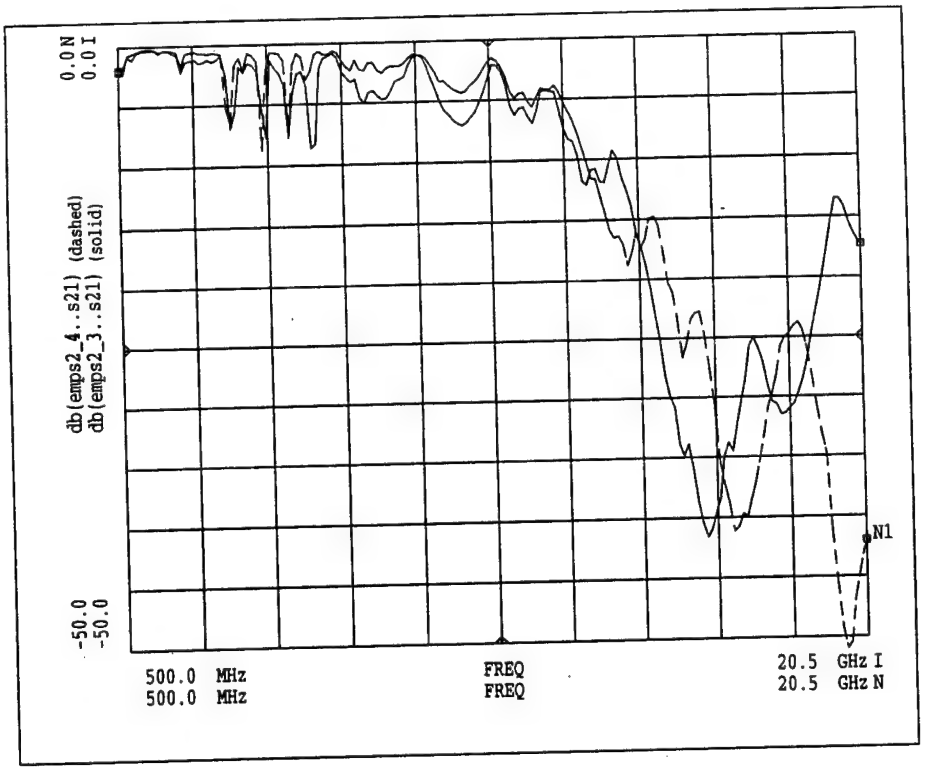


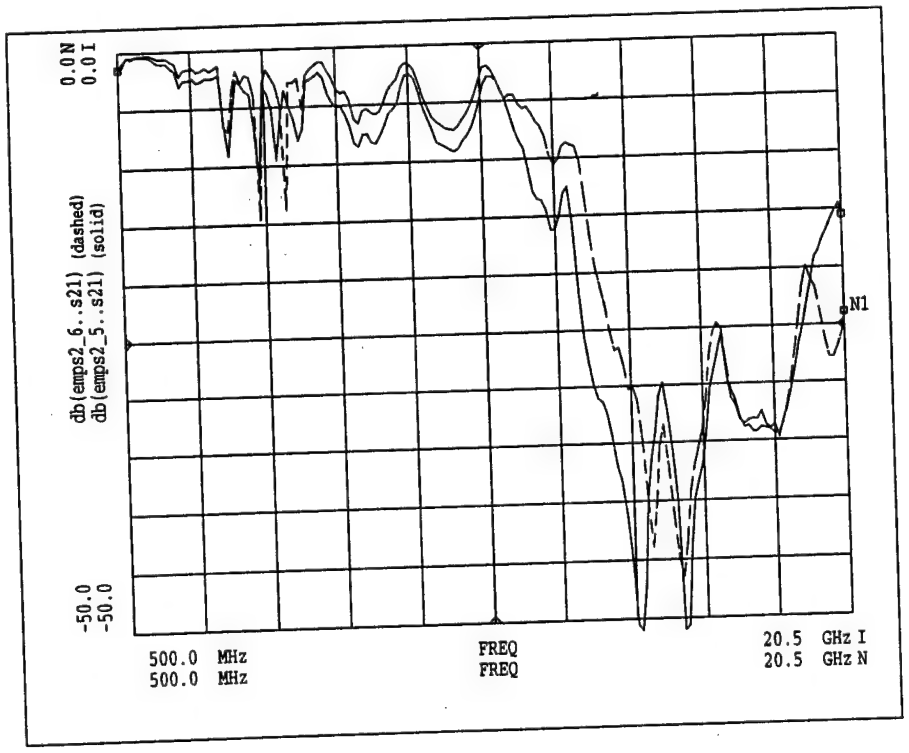
Appendix H –Diplexer Signal Combiner S21 Performance



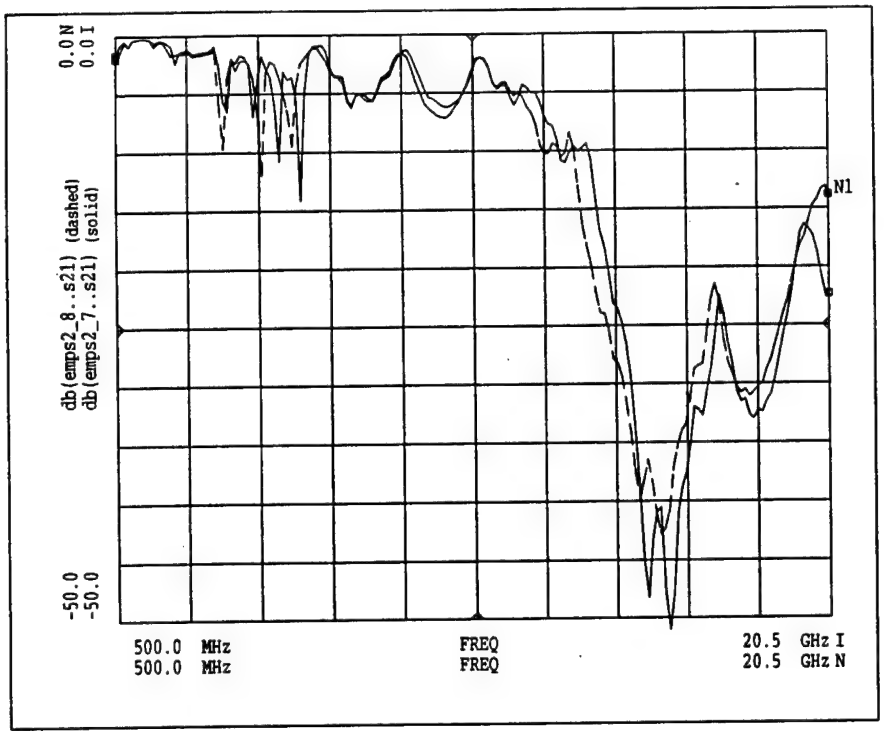


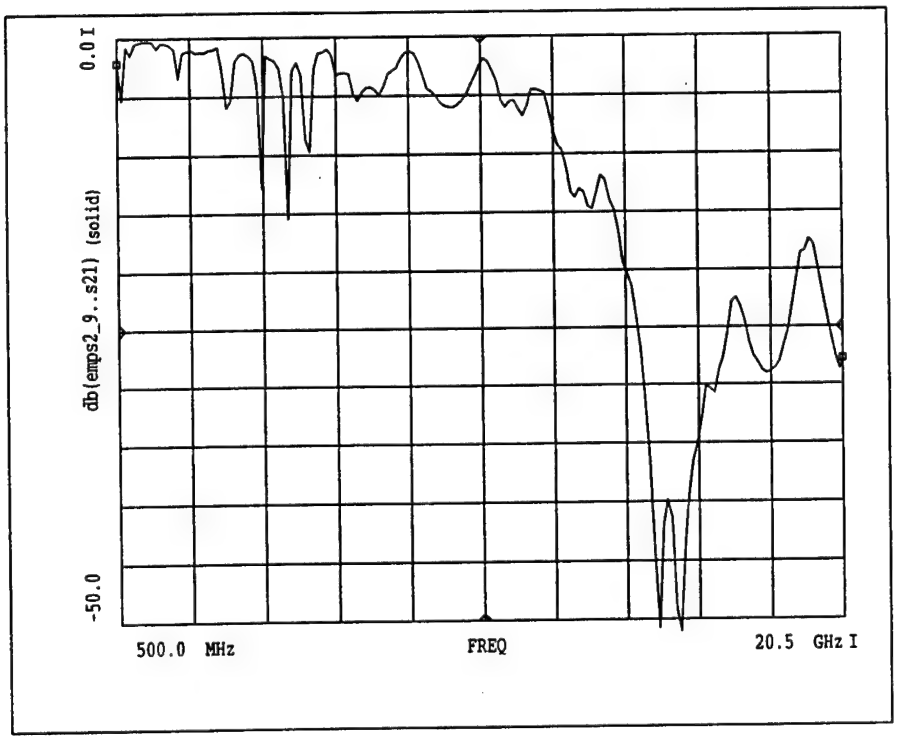
Appendix H –Diplexer Signal Combiner S21 Performance



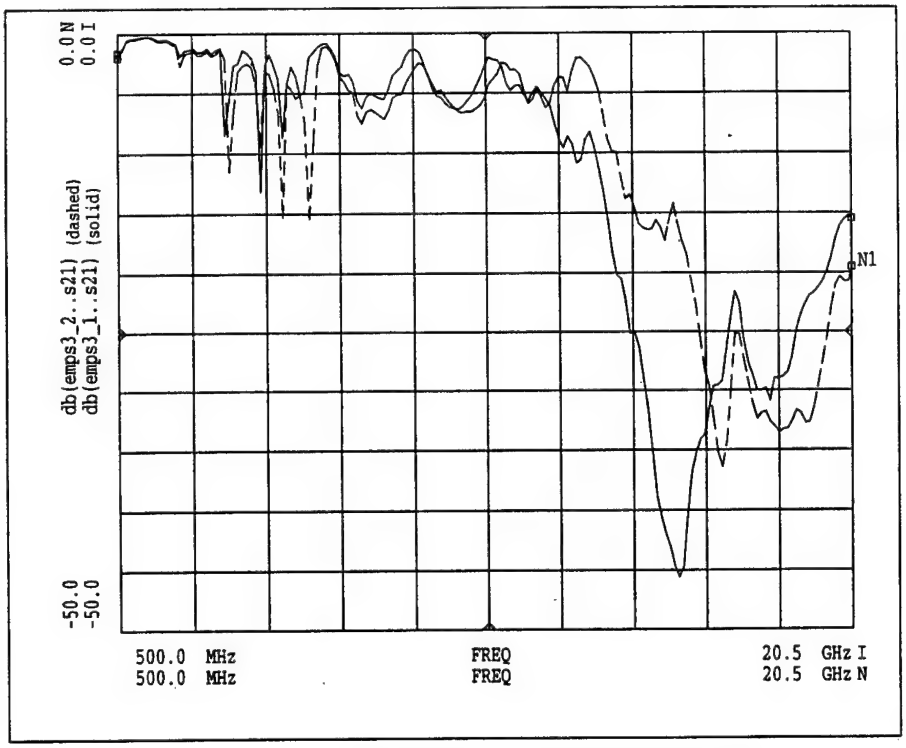


Appendix H –Diplexer Signal Combiner S21 Performance

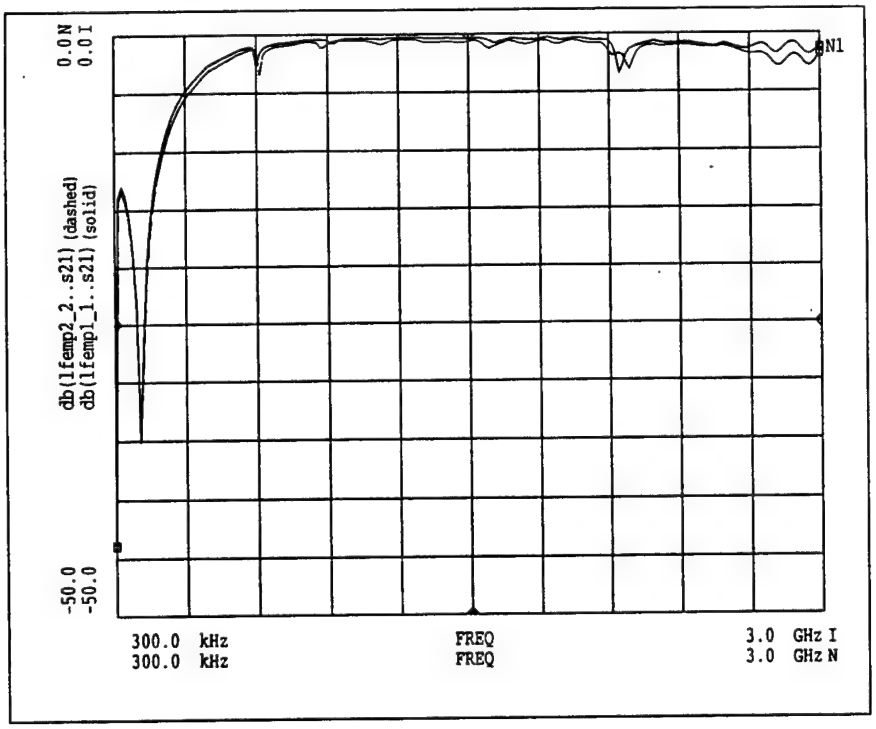


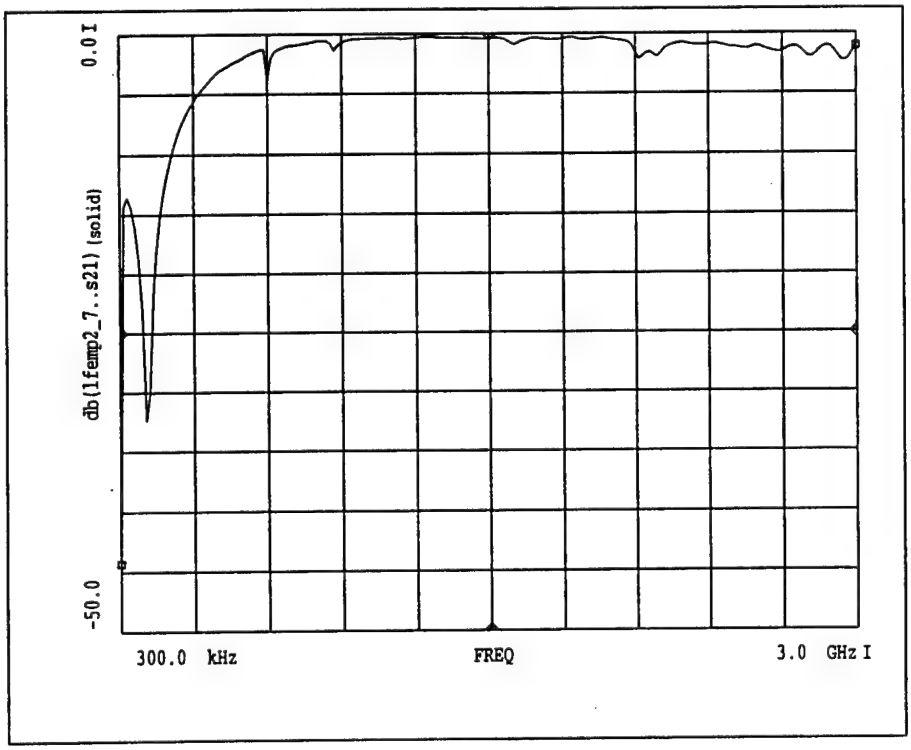


Appendix H –Diplexer Signal Combiner S21 Performance



Appendix H –Diplexer Signal Combiner S21 Performance





Appendix J: Manufacturer's Specifications of Wide-band Amplifiers

DBS Microwave Inc.

FINAL TEST DATA
AMPLIFIER MODEL

DPT-18616

S/N: 001

FREQUENCY RESPONSE	GAIN	NOISE FIGURE	P-1DB	VSWR 50 OHMS	
(GHZ)	(DB)	(DB)	(DBM)	IN	OUT
6	37.6	5.7	32.0	1.17	1.46
9	37.8	6.2	31.1	1.26	1.59
12	36.9	5.9	30.4	1.48	1.60
15	36.8	5.9	30.3	1.52	1.80
18	37.9	6.0	30.9	1.45	1.18
MIN.	36.5	--------	+30.3	--------	--------
MAX.	38.1	6.2	--------	1.59	1.83
SPEC.	32/44	10	+30	2.0	2.0

Supply Voltage +15 V

Current 2460 Spec. 2500 Typ

* All measurements taken at +25 C unless otherwise stated.

D.B.S. Microwave Inc. C-1-A. Accept 03

Technician [signature]

Date 5-15-97

Q.A. _____

Date 5/16/97

4805 Golden Foothill Parkway • El Dorado Hills, CA 95762 • 916-939-7545 Fax 916-939-7540

DBS Microwave Inc.

FINAL TEST DATA
AMPLIFIER MODEL

APT- 1616

S/N: 002

FREQUENCY RESPONSE	GAIN	NOISE FIGURE	P-1DB	VSWR 50 OHMS	
(GHZ)	(DB)	(DB)	(DBM)	IN	OUT
6	38.5	6.4	31.2	1.15	1.54
9	38.1	6.6	31.2	1.32	1.67
12	38.4	6.4	30.6	1.60	1.76
15	39.0	5.9	31.4	1.27	1.30
18	38.9	6.4	30.7	1.32	1.37
MIN.	37.7	--------	+30.6	--------	--------
MAX.	39.4	6.6	--------	1.77	1.83
SPEC.	32/44	10	+30	2.0	2.0

Supply Voltage +15 V

Current 2495 ma Spec. 2500 Typ mA.

* All measurements taken at +25 C unless otherwise stated.

Technician Rob Barnett

Date 5-15-97

Q.A. _____

Date 5/16/97

4805 Golden Foothill Parkway • El Dorado Hills, CA 95762 • 916-939-7545 Fax 916-939-7540

DBS Microwave Inc.

FINAL TEST DATA
AMPLIFIER MODEL

DBP 0206 N533

S/N: 012

FREQUENCY RESPONSE	GAIN	NOISE FIGURE	P-1DB	VSWR 50 OHMS	
(GHZ)	(DB)	(DB)	(DBM)	IN	OUT
2.0	34.4	6.6	33.1	1.9	2.1
3.0	35.7	6.4	33.7	1.1	2.0
4.0	34.5	6.3	34.0	1.1	1.8
5.0	33.0	6.3	33.2	1.2	1.6
6.0	32.8	6.2	33.0	1.3	1.8
MIN.	32.8	--------	33.0	--------	--------
MAX.	35.7	6.6	--------	1.9	2.1
SPEC.	30-38	7.0	33.0	2.2	2.2

Supply Voltage 15 V

Current 1998 mA Spec. 2000 mA

* All measurements taken at +25 C unless otherwise stated.

Technician [signature] Q.A. [signature]

Date 6-9-97 Date 6/10/97

4805 Golden Foothill Parkway • El Dorado Hills, CA 95762 • 916-939-7545 Fax 916-939-7540

DBS Microwave Inc.

FINAL TEST DATA
AMPLIFIER MODEL

DBP 0206 N533

S/N: 013

FREQUENCY RESPONSE	GAIN	NOISE FIGURE	P-1DB	VSWR 50 OHMS	
(GHZ)	(DB)	(DB)	(DBM)	IN	OUT
2.0	35.9	6.2	33.8	2.0	2.0
3.0	36.4	5.9	33.3	1.5	2.0
4.0	35.0	5.9	34.0	1.7	1.8
5.0	34.8	6.0	33.6	1.7	1.6
6.0	35.8	5.9	34.0	2.0	1.6
MIN.	34.8	--------	33.3	--------	--------
MAX.	36.4	6.2	--------	2.0	2.0
SPEC.	30-38	7.0	33.0	2.2	2.2

Supply Voltage 15 V

Current 1999 mA Spec. 2000 mA

* All measurements taken at +25 C unless otherwise stated.

Q.A. QA Accept 03

Technician

Date 6-9-97

Date 6/10/97

4805 Golden Foothill Parkway • El Dorado Hills, CA 95762 • 916-939-7545 Fax 916-939-7540

CERNEX, Inc.

Solid State Amplifier Test Data Sheet

Customer: ***Temperature: +25° C***

Serial #: 2346 ***Model # CPA02063230***

Specifications ***Measured data***

Frequency (GHz)	2-6	2	4	6
SS Gain (db) (min)	32	44.3	45.2	44.8
Gain Flatness (db) (max)	+/-1.75	+/- 1.1 dB		
P1db (dbm) (min)	30	30.9	33.3	30.8
Noise Figure ((db) (max)	5.5	< 5.5	< 5.5	< 5.5
Input VSWR (max)	2:01	2.1 : 1		
Output VSWR (max)	2:01	< 1.5 : 1		
DC Power	15V @1100mA	1000 mA		

Tested by: DN Date: 6/5/97

Q.A: QA 1 Date: JUN 06 1997

19925 Stevens Creek Blvd., Suite 126 • Cupertino, CA 95014
Tel. (408) 973-7216 • Fax (408) 252-5189

CERNEX, Inc.

Solid State Amplifier Test Data Sheet

Customer: ***Temperature: +25° C***

Serial #: 2347 ***Model # CPA02063230***

Specifications ***Measured data***

Frequency (GHz)	2-6	2	4	6
SS Gain (db) (min)	32	43.1	42.0	43.3
Gain Flatness (db) (max)	+/-1.75	+/- 1.20dB		
P1db (dbm) (min)	30	31.0	33.0	30.4
Noise Figure ((db) (max)	5.5	<5.5	<5.5	<5.5
Input VSWR (max)	2:01	2.1 : 1		
Output VSWR (max)	2:01	<1.7 : 1		
DC Power	15V @1100mA	984 mA		

Tested by: DN Date: 6/6/97

Q.A: QA 1 Date: JUN 06 1997

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CERNEX, Inc.

Solid State Amplifier Test Data Sheet

Customer: ***Temperature: +25° C***

Serial #: 2348 ***Model # CPA02063230***

Specifications		***Measured data***		
Frequency (GHz)	**2-6**	**2**	**4**	**6**
SS Gain (db) (min)	**32**	42.2	40.6	41.8
Gain Flatness (db) (max)	**+/-1.75**	+/- 1.2 dB		
P1db (dbm) (min)	**30**	30.9	33.2	30.3
Noise Figure ((db) (max)	**5.5**	< 5.5	< 5.5	< 5.5
Input VSWR (max)	**2:01**	2.0 : 1		
Output VSWR (max)	**2:01**	< 1.7 : 1		
DC Power	**15V @1100mA**	1050 mA		

Tested by: DDJ **Date:** 6/6/97

Q.A: QA 1 **Date:** JUN 0 6 1997

19925 Stevens Creek Blvd., Suite 126 • Cupertino, CA 95014
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DBS Microwave Inc.

FINAL TEST DATA
AMPLIFIER MODEL

DBP-0102N533

S/N: 007

FREQUENCY RESPONSE (GHZ)	GAIN (DB)	NOISE FIGURE (DB)	P-1DB (DBM)	VSWR 50 OHMS IN	VSWR 50 OHMS OUT
0.5	42.6	3.1	33.2	1.2	1.7
1.0	44.6	2.9	33.4	1.7	1.3
1.5	42.0	2.9	33.3	1.8	1.3
2.0	42.4	2.9	33.9	1.7	1.4
MIN.	41.7	--------	33.2	--------	--------
MAX.	45.2	3.1	--------	1.8	1.7
SPEC.	40.0 min. - 300 max.	5.5	33.0	2.2	2.2

Supply Voltage +15 V

Current 1120 mA Spec. 1400mA Max.

* All measurements taken at +25 C unless otherwise stated.

Technician Bill Brathaus

Q.A. _____

Date 5/19/97

Date 5/20/97

4805 Golden Foothill Parkway • El Dorado Hills, CA 95762 • 916-939-7545 Fax 916-939-7540

DBS Microwave Inc.

FINAL TEST DATA
AMPLIFIER MODEL

DBP-0102N533

S/N: 008

FREQUENCY RESPONSE	GAIN	NOISE FIGURE	P-1DB	VSWR 50 OHMS	
(GHZ)	(DB)	(DB)	(DBM)	IN	OUT
0.5	43.4	3.1	33.3	1.2	1.5
1.0	45.6	2.9	33.5	1.7	1.3
1.5	43.5	2.9	34.0	1.8	1.3
2.0	44.2	3.0	34.2	1.6	1.4
MIN.	43.3	--------	33.3	--------	--------
MAX.	46.2	3.1	--------	1.8	1.5
SPEC.	40.0 Min. - 50.0 Max.	5.5	33.0	2.2	2.2

Supply Voltage +15 V

Current 1180 mA Spec. 1400 mA Max.

* All measurements taken at +25 C unless otherwise stated.

Technician Bill Greathouse

Date 5/19/97

Q.A. _____

Date 5/20/97

4805 Golden Foothill Parkway • El Dorado Hills, CA 95762 • 916-939-7545 Fax 916-939-7540

DBS Microwave Inc.

FINAL TEST DATA
AMPLIFIER MODEL

DBP-0102N533

S/N: 009

FREQUENCY RESPONSE	GAIN	NOISE FIGURE	P-1DB	VSWR 50 OHMS	
(GHZ)	(DB)	(DB)	(DBM)	IN	OUT
0.5	42.9	3.2	33.8	1.2	1.4
1.0	44.0	2.9	33.7	1.6	1.3
1.5	41.9	3.0	34.1	1.8	1.3
2.0	43.0	3.0	34.3	1.7	1.4
MIN.	41.6	--------	33.7	--------	--------
MAX.	44.7	3.2	--------	1.8	1.4
SPEC.	40.0 Min. - 50.0 Max.	5.5	33.0	2.2	2.2

Supply Voltage +15 V

Current 1170 mA Spec. 1400mA Max.

* All measurements taken at +25 C unless otherwise stated.

D.B.S. Microwave Quality Q.A. Accept 03

Technician Bill Greathouse Q.A. _____

Date 5/19/97 Date 5/20/97

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DBS Microwave Inc.

FINAL TEST DATA
AMPLIFIER MODEL

DBP-0102N533

S/N: 010

FREQUENCY RESPONSE	GAIN	NOISE FIGURE	P-1DB	VSWR 50 OHMS	
(GHZ)	(DB)	(DB)	(DBM)	IN	OUT
0.5	42.6	3.2	33.2	1.2	2.2
1.0	44.4	2.9	33.7	1.6	1.3
1.5	42.4	3.0	34.2	1.8	1.3
2.0	42.2	3.0	33.9	1.7	1.3
MIN.	42.0	--------	33.2	--------	--------
MAX.	45.0	3.2	--------	1.9	2.2
SPEC.	40.0 Min. - 50.0 Max.	5.5	33.0	2.2	2.2

Supply Voltage +15 V

Current 1140 mA Spec. 1400 mA Max.

* All measurements taken at +25 C unless otherwise stated.

DBS Microwave Dallas QA Accept 03

Technician Bill Braithwaite

Date 5/19/97

Q.A. _____

Date 5/20/97

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